MESSRS.客戶公司行號

SPECIFICATION FOR APPROVAL

承 認 書

Product	**IC**
Part No.	**LY8322**
Customer Approval	
Customer Part No.	

Approved By	Checked By	Made By
工程部 JASON CHEN MAY-28-2015	工程部 ZACK KUO MAY-28-2015	工程部 ZACK KUO MAY-28-2015

Advanced Acoustic Technology Corporation

昊宬股份有限公司//常州笠翔电子有限公司

ISO 9001 Certified

ISO 14001 Certified

QS9000 Certified

Head Company / 2F, No.207, Sec. 6, Chung Shan N. Rd., Taipei, Taiwan

Tel: +886-2-8866-5255 Fax: +886-2-8866-5250

大陸總公司 / 中國江蘇省常州市新北區龍虎塘工業園新苑四路 89 號

Tel: +86-519-8511-2382 Fax: +86-519-8510-0908

http://www.aatc.com.tw www.aatc.com.cn

EDITION:1.1

ADVANCED ACOUSTIC TECHNOLOGY CORP.
昊 宬 股 份 有 限 公 司

REVISIONS			
PRODUCT			**IC**
PART NO.			**LY8322**
REV.	**REVISER**	**DATE**	**DESCRIPTION**
1	**ZACK**	2015-05-28	Creating new drawing SPEC.

Lyontek Inc.

LY8322

Preliminary Rev. 0.9

20Wx2(BTL) Stereo / 40Wx1(PBTL) Mono Class D Audio Amplifier with Filter Free

FEATURES

- High output power capability:
  (Test @1KHz,THD+N=10%.25℃)

R_{Load}	4Ω	8Ω
SEx4	4.5Wx4/12V	2.5Wx4/12V
	11Wx4/19V	6.3Wx4/19V
BTLx2	6Wx2/7.4V	3.5Wx2/7.4V
	8Wx2/8.4V	4.5Wx2/8.4V
	16.5Wx2/12V	9.5Wx2/12V
	20Wx2/19V	24.5Wx2/19V
R_{Load}	4Ω	2Ω
PBTLx1	40Wx1/19V	40Wx1/12V

- 7V ~ 24V power supply.
- Differential or Single-end inputs.
- 4 kinds of output type options:
  4xSE、2xBTL、2.1CH.(2xSE+1xBTL)、1xPBTL
- L/C filter-free operation
- Adjustable Power Limiter Speaker Protection.
- Short-Circuit protection with automatic recovery.
- Over-Heat protection with automatic recovery.
- Under-voltage and Over-voltage detection.
- Mute function selectable.
- 4 selectable, fixed gain settings.
  (20dB，26dB，32dB，36dB)
- Green package available.
- Space saving package :
  28-pin TSSOP 173mil package.

GENERAL DESCRIPTION

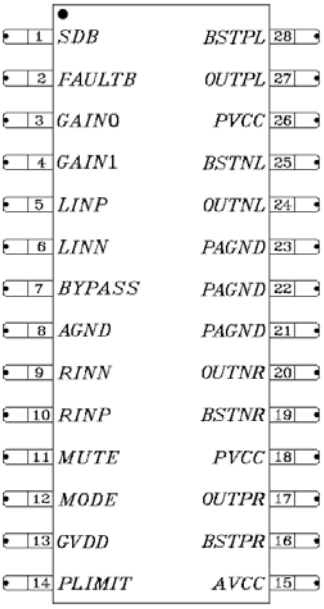
The LY8322 is a high efficiency class D audio power amplifier. It can to work either in dual bridge、quad single-ended output 、2.1 channel and PBTL mono application configuration. The device use advanced EMI suppression technology enables the use low cost ferrite-bead filters at the outputs while meeting EMC requirements.
The outputs are also fully protected against short to PVDD or GND and output-to-output pin.
The short-circuit protection and thermal protection include an auto-recovery feature.
The device features a low noise and a low power consumption in shutdown mode. It also utilizes circuitry to reduce low noise during device turn-on.

APPLICATION

- Sound-bar Home Theater.
- Powered Speakers.
- Music instrument devices.
- Multimedia TFT LCD TVs / Monitors.

PIN CONFIGURATION

LY8322 TSSOP28 pin configuration (TOP VIEW)



5F, No. 2, Industry E . Rd. IX, Science-Based Industrial Park, Hsinchu 300, Taiwan
TEL: 886-3-6668838
FAX: 886-3-6668836

PIN DESCRIPTION

SYMBOL	Pin No.	DESCRIPTION
SDB	1	Shutdown control pin.(when **LOW** level in shutdown mode).
FAULTB	2	Open drain output used to display short circuit status. Voltage compliant to GVDD. Short circuit faults can be set to auto-recovery by connecting FAULT pin to SD pin. Short circuit faults must be reset by cycling PVCC or MCU.
GAIN0	3	Gain select pin.
GAIN1	4	Gain select pin.
LINP	5	Positive(+) L channel audio input.
LINN	6	Negative(-) L channel audio input.
BYPASS	7	Bypass pin.
AGND	8	Analog GND.
RINN	9	Negative(-) R channel audio input.
RINP	10	Positive(+) R channel audio input.
MUTE	11	Mute signal for quick enable/disable of output. ((When **HIGH** (connect to GVDD) level in mute mode).
MODE	12	Output mode selectable.
GVDD	13	High-side FET gate drive supply. Nominal voltage is 6.9V.
PLIMIT	14	Power limit level adjust. Connect a resistor divider from AVCC to set power limit voltage.
AVCC	15	Analog Power supply.
BSTPR	16	Bootstrap I/O for Positive(+) R channel.
OUTPR	17	Speaker output for Positive(+) R channel.
PVCC	18/26	Power supply of R、L channel.
BSTNR	19	Bootstrap I/O for Negative(-) R channel.
OUTNR	20	Speaker output for Negative(-) R channel.
PGND	21/22/23	Ground of R、L channel.
OUTNL	24	Speaker output for Negative(-) L channel.
BSTNL	25	Bootstrap I/O for Negative(-) L channel.
OUTPL	27	Speaker output for Positive(+) L channel.
BSTPL	28	Bootstrap I/O for Positive(+) L channel.

▪ ORDERING INFORMATION

Ordering Code	Speaker Channels	Pin/ Package	Output Power (THD+N=10%)(*3)			Input Type	Output Type
LY8322A	Multi channel	TSSOP28	R_{Load}	4Ω	8Ω	Single-End / Differential	SEx4(*4) 2xBTL 2.1CH 1xPBTL
			SEx4	4.5Wx4/12V	2.5Wx4/12V		
				11Wx4/19V	6.3Wx4/19V		
			BTLx2	6Wx2/7.4V	3.5Wx2/7.4V		
				8Wx2/8.4V	4.5Wx2/8.4V		
				16.5Wx2/12V	9.5Wx2/12V		
				20Wx2/19V(*5)	24.5Wx2/19V		
			R_{Load}	4Ω	2Ω		
			PBTLx1	40Wx1/19V	40Wx1/12V		

(*3) The device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.
For best performance, when driving≧14V/4Ω power and loading, the PLIMIT pin must control to 2.0V voltage. If the device added external heat sink, the PLIMIT pin must control to 1.2V voltage.
(*4) If Output type select SEx4, The audio input must use Single-End type.
(*5) PLIMIT Voltage = 2.0V

▪ DEMO BOARD ORDERING INFORMATION

Demo Board Ordering Code	Pin/ Package	Input Type	Speaker Output Channels	Notes
LY8322A-DB1	TSSOP28	Single-End / Differential	PBTL mode (Mono)	
LY8322A-DB2			BTLx2 mode (Stereo)	
LY8332A-DB3			2.1CH mode (SEx2+BTLx1)	
LY8332A-DB4			SEx4 mode	

TYPICAL APPLICATION CIRCUIT

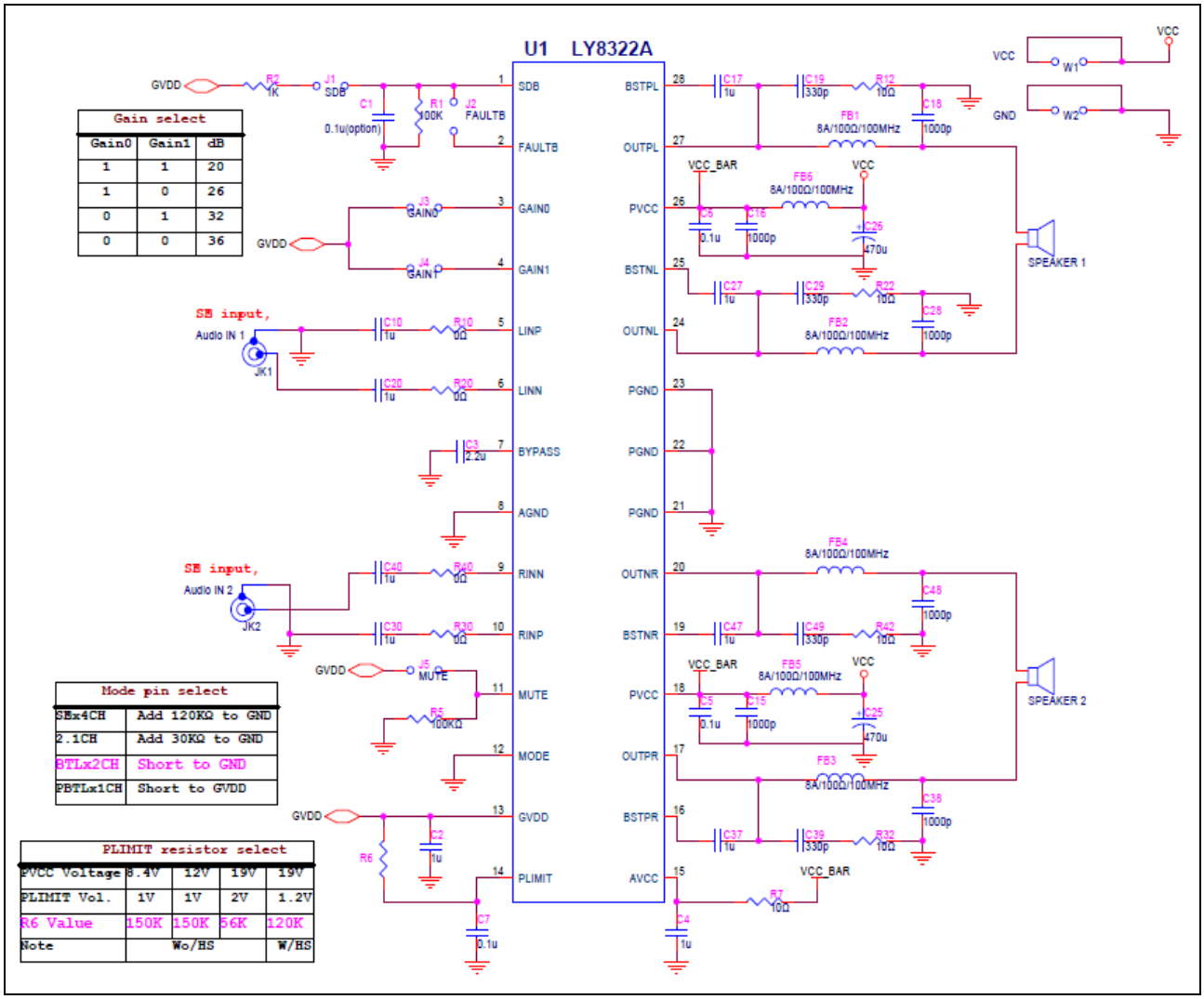


Figure 1. LY8322 Application Circuit with BTLx2 Schematic

(*3) The device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.
For best performance, when driving≧14V/4Ω power and loading, the PLIMIT pin must control to 2.0V voltage. If the device added external heat sink, the PLIMIT pin must control to 1.2V voltage.

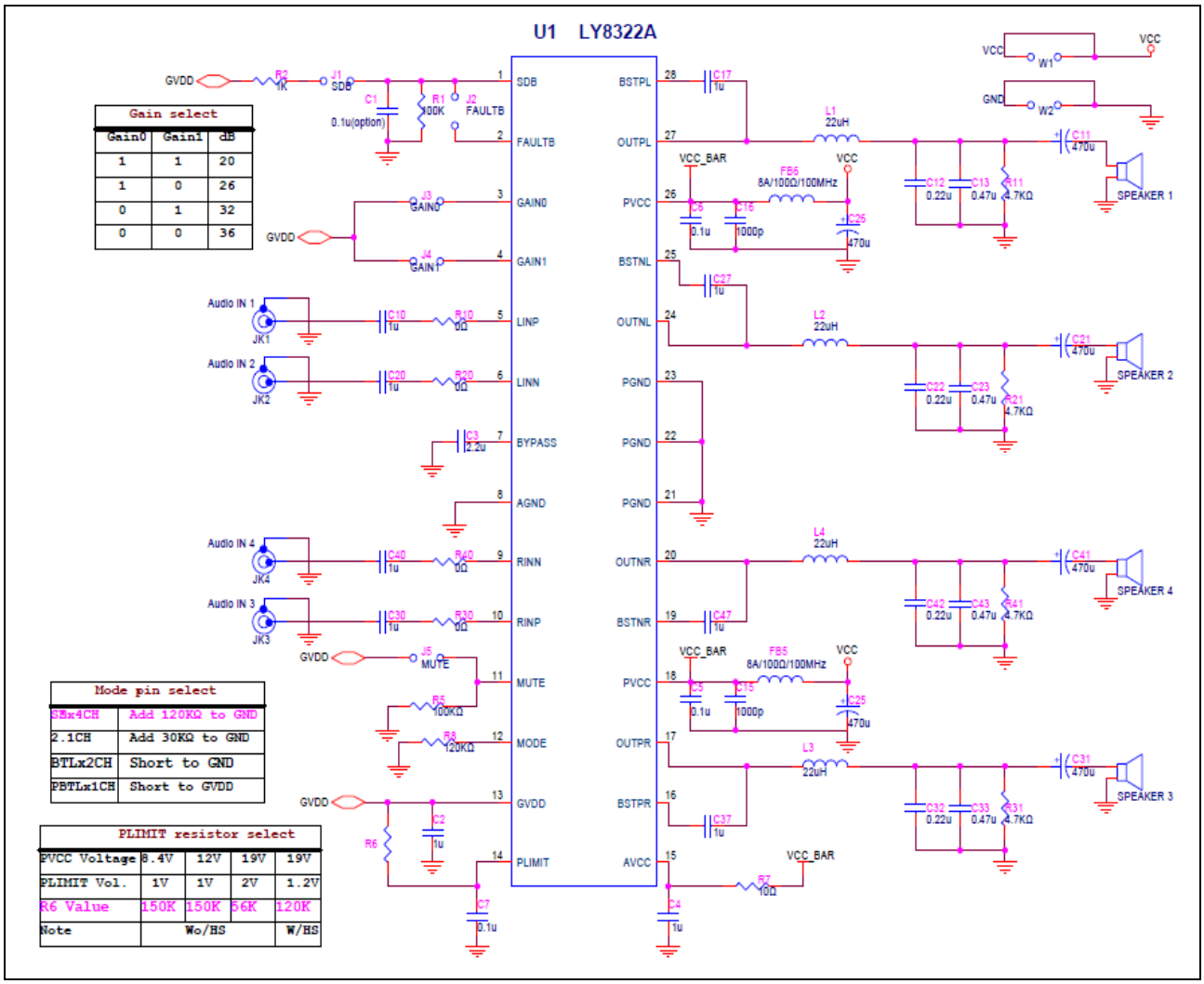


Figure 2. LY8322 Application Circuit with SEx4 Schematic

(*3) The device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.
For best performance, when driving≧14V/4Ω power and loading, the PLIMIT pin must control to 2.0V voltage. If the device added external heat sink, the PLIMIT pin must control to 1.2V voltage.

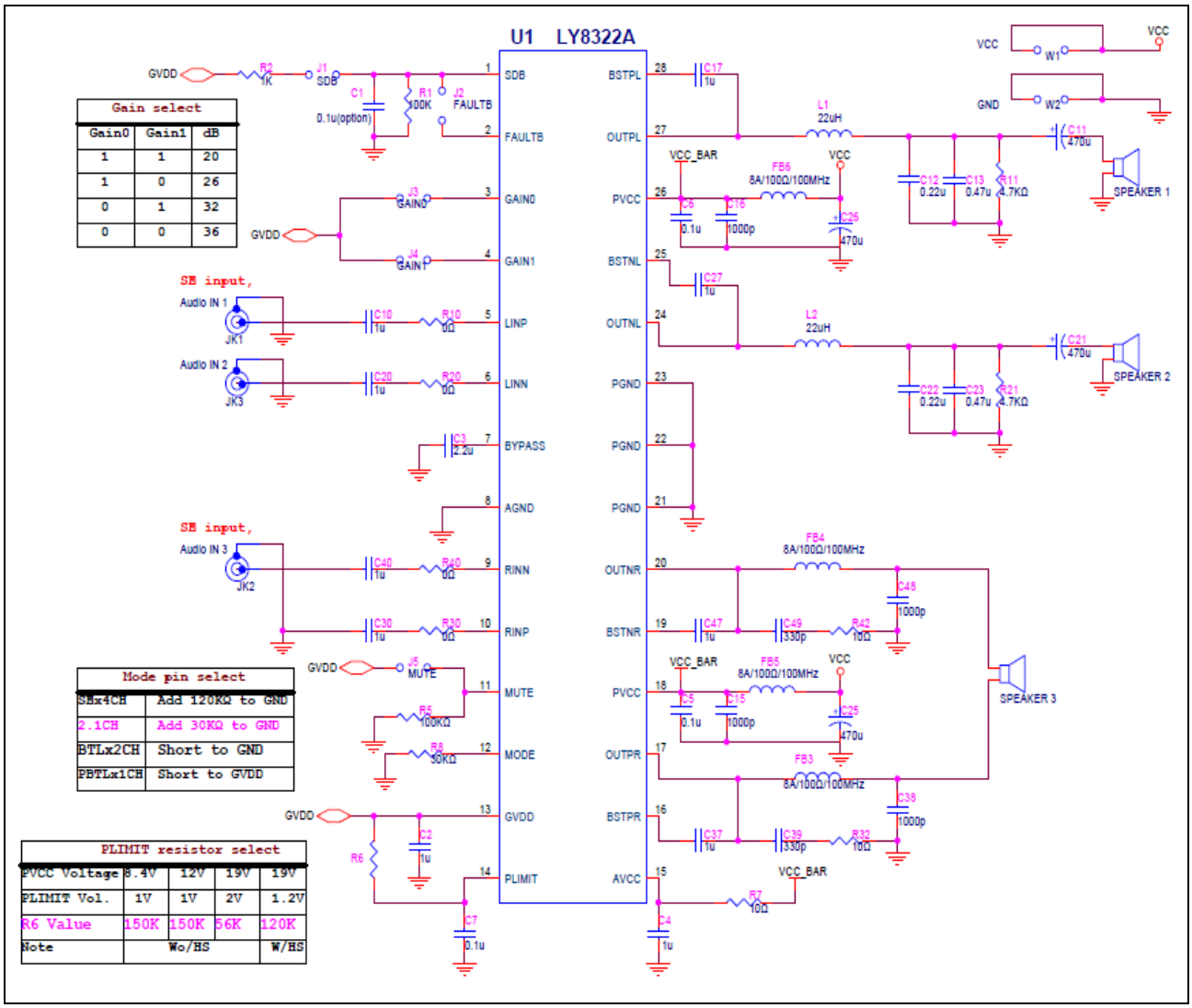


Figure 3. LY8322 Application Circuit with 2.1CH (SEx2 + BTLx1) Schematic

(*3) The device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.
For best performance, when driving≧14V/4Ω power and loading, the PLIMIT pin must control to 2.0V voltage. If the device added external heat sink, the PLIMIT pin must control to 1.2V voltage.

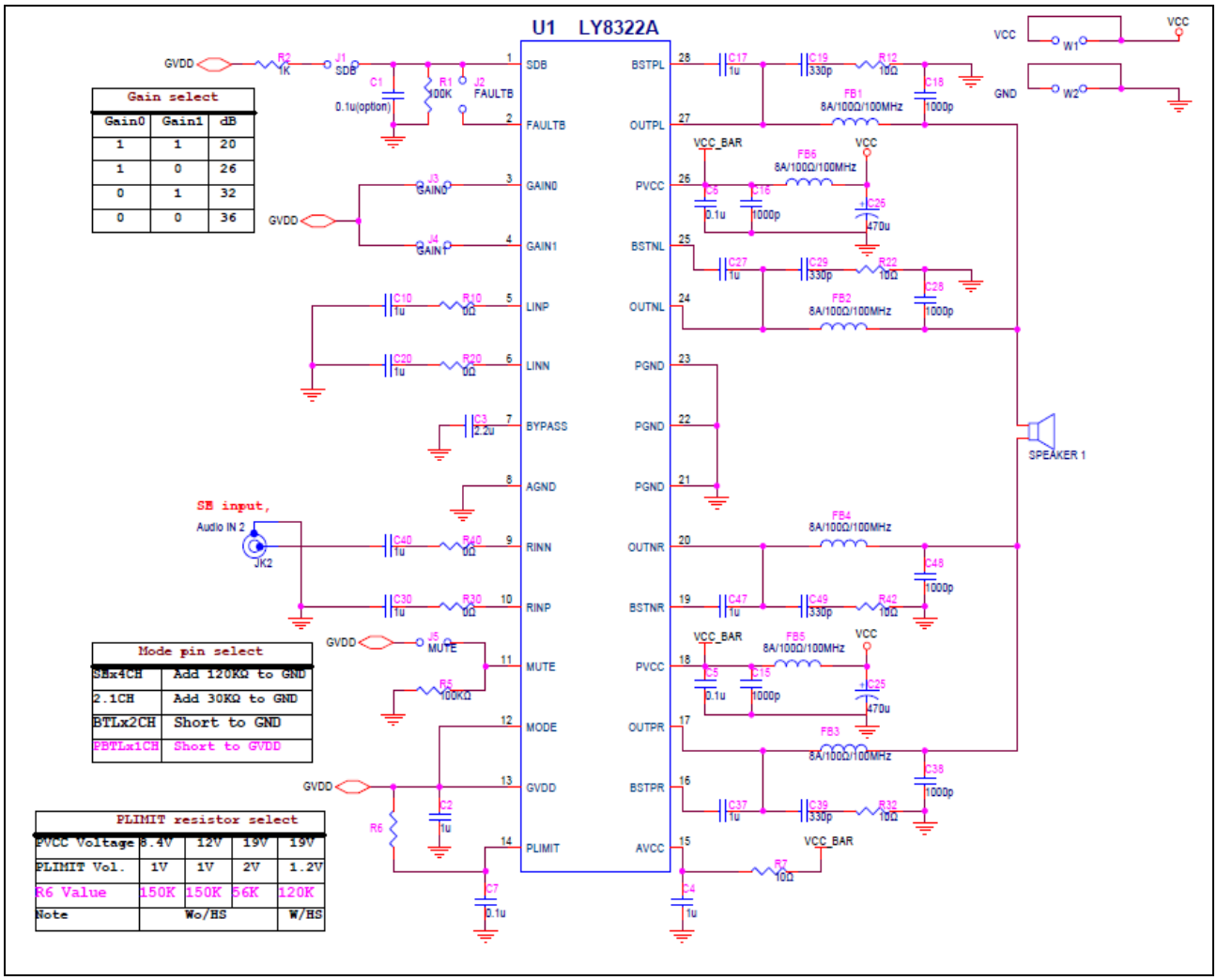


Figure 4. LY8322 Application Circuit with PBTLx1 Schematic

(*3) The device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.
For best performance, when driving≧14V/4Ω power and loading, the PLIMIT pin must control to 2.0V voltage. If the device added external heat sink, the PLIMIT pin must control to 1.2V voltage.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	PVCC	28	V
Operating Temperature	T_A	-40 to 85 (I grade)	℃
Input Voltage	V_I	-0.3V to PVCC +0.3V	V
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	Internally Limited	W
ESD Susceptibility	V_{ESD}	2000	V
Junction Temperature	T_{JMAX}	150	℃
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	℃

ELECTRICAL CHARACTERISTICS (1) (T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *2	MAX.	UNIT
Power supply voltage	PVCC	PVCC, AVCC		7	-	24	V
Oscillator frequency	fOSC			-	345	-	KHz
High-level input voltage	V_{IH}	SDB, MUTE		2	-	-	V
Low-level input voltage	V_{IL}	SDB, MUTE		-	-	0.3	V
Quiescent Current	I_Q	SD≧2.0V, MUTE=0V, No Load,BTL Mode.	P_{VCC}=7.4V	-	33	-	mA
			P_{VCC}=8.4V	-	35	-	
			P_{VCC}=12V	-	42	-	
			P_{VCC}=19V	-	58	-	
			P_{VCC}=24V	-	83	-	
Quiescent Current (in Mute Mode)		SD≧2.0V, MUTE≧2.0V, No Load,BTL Mode.	P_{VCC}=7.4V	-	29	-	
			P_{VCC}=8.4V	-	32	-	
			P_{VCC}=12V	-	40	-	
			P_{VCC}=19V	-	58	-	
			P_{VCC}=24V	-	81	-	
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$≦0.8V,No Load	P_{VCC}=7.4V	-	66	-	uA
			P_{VCC}=8.4V	-	71	-	
			P_{VCC}=12V	-	88	-	
			P_{VCC}=19V	-	125	-	
			P_{VCC}=24V	-	157	-	
Gain	G	Gain0=0	Gain1=0	-	36	-	dB
			Gain1=1	-	32	-	
		Gain0=1	Gain1=0	-	26	-	
			Gain1=1	-	20	-	
Gate Drive supply	GVDD	GVDD current=58.7uA		-	6.87	-	V
Bypass output voltage	V_{BYPASS}	Pvcc=7~24V,		-	2.9	-	V
Output offset voltage	|V_{OS}|	V_I=0V, Gain=20dB, BTL Mode	P_{VCC}=12V	-	55	-	mV
Thermal shutdown temperature	T_{SD}	Shutdown temp.		-	165	-	℃
		Restore temp.		-	110	-	
Mute attenuation		Gain=20dB, 1W=0dB	P_{VCC}=8.4V	-	-82	-	dB
			P_{VCC}=12V	-	-79	-	
			P_{VCC}=19V	-	-75	-	
Mute delay	Δt mute	Time from mute input switches high until outputs muted. BTL mode	P_{VCC}=8.4V	-	14	-	us
			P_{VCC}=12V	-	14	-	
			P_{VCC}=19V	-	9	-	
Unmute delay	Δt unmute	Time from mute input switches low until outputs muted. BTL mode	P_{VCC}=8.4V	-	12	-	
			P_{VCC}=12V	-	15	-	
			P_{VCC}=19V	-	9	-	
Start-up time from shutdown	Z_I	Ci=1uF, BTL mode. Pvcc=7~24V	C_{bypass}=0.1μF	-	70	-	ms
			C_{bypass}=0.47μF	-	250	-	
			C_{bypass}=1μF	-	950	-	
			C_{bypass}=2.2μF	-	1	-	s
			C_{bypass}=4.7μF	-	1.2	-	

(*2) Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at PVCC = PVCC(TYP.) and T_A = 25℃

▪ OPERATING CHARACTERISTICS (2)(TA = 25℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *2	MAX.	UNIT
Supply ripple rejection	Ksvr	Gain=20, RL=4Ω, BTL mode Vripple = 200mVpp at 1kHz, Input=GND, f=217Hz	PVCC=8.4V	-	-77.5	-	dB
			PVCC=12V	-	-76	-	
			PVCC=19V	-	-78	-	
Output voltage noise	Vn	**BTL Mode**, input=SE mode, Gain=20dB, A-weighting, f=20Hz to 20kHz,RL=4Ω,	PVCC=8.4V	-	370	-	uV
			PVCC=12V	-	388	-	
			PVCC=19V	-	422	-	
Signal-to-noise ratio	SNR	**BTL Mode**, input=SE mode, Gain=20dB, RL=4Ω, f=1kHz, 1W=0dB	PVCC=8.4V	-	-74.6	-	dB
			PVCC=12V	-	-74.2	-	
			PVCC=19V	-	-73.5	-	
Crosstalk	Cs	**BTL Mode**, input=SE mode, Gain=20dB, RL=4Ω, f=1KHz, Po=1W, L to R,	PVCC=8.4V	-	-75	-	dB
			PVCC=12V	-	-75	-	
			PVCC=19V	-	-75	-	
		BTL Mode, input=SE mode, Gain=20dB, RL=4Ω, f=1KHz, Po=1W, R to L,	PVCC=8.4V	-	-74	-	
			PVCC=12V	-	-76	-	
			PVCC=19V	-	-77	-	

(*2) Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at PVCC = PVCC(TYP.) and TA = 25℃

▪ OPERATING CHARACTERISTICS (3)(TA = 25℃)

SE Mode Output Power

PARAMETER	SYMBOL	Voltage	RL=4Ω *2				RL=8Ω*2			
			1 Channel		4 Channel		1 Channel		4 Channel	
			10%	1%	**10%**	1%	**10%**	1%	**10%**	1%
		7V	1.5	1.3	1.5	1.2	0.9	0.7	0.8	0.7
		7.4V	1.8	1.4	1.7	1.3	1	0.8	0.9	0.7
		8V	2.1	1.7	2	1.6	1.1	0.9	1.1	0.9
		8.4V	2.4	1.9	2.1	1.7	1.3	1	1.2	0.9
		9V	2.7	2.2	2.5	2	1. 5	1.2	1.4	1.2
		10V	3.3	2.6	3	2.3	1.8	1. 5	1.7	1.4
		12V	4.7	3.8	4.5	3.4	2.5	2.1	2.5	2.1
		14V	6.4	5.2	6	4.3	3.5	2.8	3.4	2.7
		16V	7.3	5.8	7.8	6.2	4.6	3.7	4.4	3.5
		18V	8.4	6.6	10	7.6	5.9	4.6	5.7	4.4
		19V	10.6	8.5	11.2	9.1	6.5	5.2	6.3	5.1
		20V	13.2*3	10.3*3	12.3*3	9.4*3	7.2	5.7	7	5.4
		22V	16*3	12.3*3	15*3	11.3*3	8.8	6.7	8.5	6.7
		24V	18.6*3	14.5*3	17.6*3	13.6*3	10.5	7.9	10.2	7.7

20Wx2(BTL) Stereo / 40Wx1(PBTL) Mono Class D Audio Amplifier with Filter Free

BTL Mode (Stereo) Output Power

PARAMETER	SYMBOL	Voltage	R_L=4Ω*2				R_L=8Ω*2			
			1 Channel		2 Channel		1 Channel		2 Channel	
			10%	1%	**10%**	1%	**10%**	1%	**10%**	1%
		7V	5.9	4.8	5.7	4.7	3.4	2.9	3.3	2.7
		7.4V	6.7	5.6	6.4	5.3	3.7	3.1	3.7	3
		8V	7.8	6.6	7.5	6.2	4.4	3.6	4.3	3.5
		8.4V	8.5	6.8	8.2	6. 7	4.8	4	4.7	4
		9V	9.8	8	9.4	7.8	5.6	4.7	5.5	4.7
		10V	12	10	11.6	9.4	6.8	5.7	6.7	5.6
		12V	17.5	14.5	16.7	13.8	10	8	9.7	7.9
		14V	23.5*3	19.5*3	22.5*3	18.3*3	13.5	11	13	11
		16V	31*3	25*3	29*3	24.5*3	18	15	17	14.5
		18V	38.5*3	32*3	36*3	29.5*3	22	18	22	18
		19V	43*3	34.5*3	40*3	33.5*3	25	21	24.5	20
		20V	47*3	39*3	43*3	35.5*3	28	23	27	22
		22V	-	-	-	-	33*3	28*3	32.5*3	27*3
		24V	-	-	-	-	39*3	33*3	38*3	32*3

PBTL Mode (Mono) Output Power

PARAMETER	SYMBOL	Voltage	R_L=2Ω*2		R_L=3Ω*2		R_L=4Ω*2		R_L=8Ω*2	
			10%	1%	**10%**	1%	**10%**	1%	**10%**	1%
		7V	10.5	8.5	8	6	6	5	3.5	2.8
		7.4V	12	10	9	7	7	5.5	3.8	3
		8V	13	11.5	10.5	8.5	8	6.8	4.5	3.5
		8.4V	15.5	12.5	11.5	9	9	7	5	4
		9V	17.5	14.5	13.5	10.5	10.5	8.5	5.7	4.7
		10V	21	17	16.5	13.5	13	10.5	7	5.7
		12V	30	24	23	19	18.5	15.5	10	8
		14V	40*3	33.5*3	31.5	26	25	20	14	11.5
		16V	-	-	41*3	33*3	33	25	18	14.5
		18V	-	-	-	-	42*3	35*3	23	19
		20V	-	-	-	-	-	-	28.5	23
		22V	-	-	-	-	-	-	34.5	27.5
		24V	-	-	-	-	-	-	41*3	32.5*3

(*2) Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at PVCC = PVCC(TYP.) and T_A = 25℃.
The test machine : Audio Precision SYS-2712A and AUX-0025.

(*3) The device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.
For best performance, when driving≧14V/4Ω power and loading, the PLIMIT pin must control to 2.0V voltage. If the device added external heat sink, the PLIMIT pin must control to 1.2V voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5
THD+N vs. Output Power (@ Output type=BTL Mode, **RL=4Ω**, f=1kHz, Gain=20dB, 2 Channel.Test)

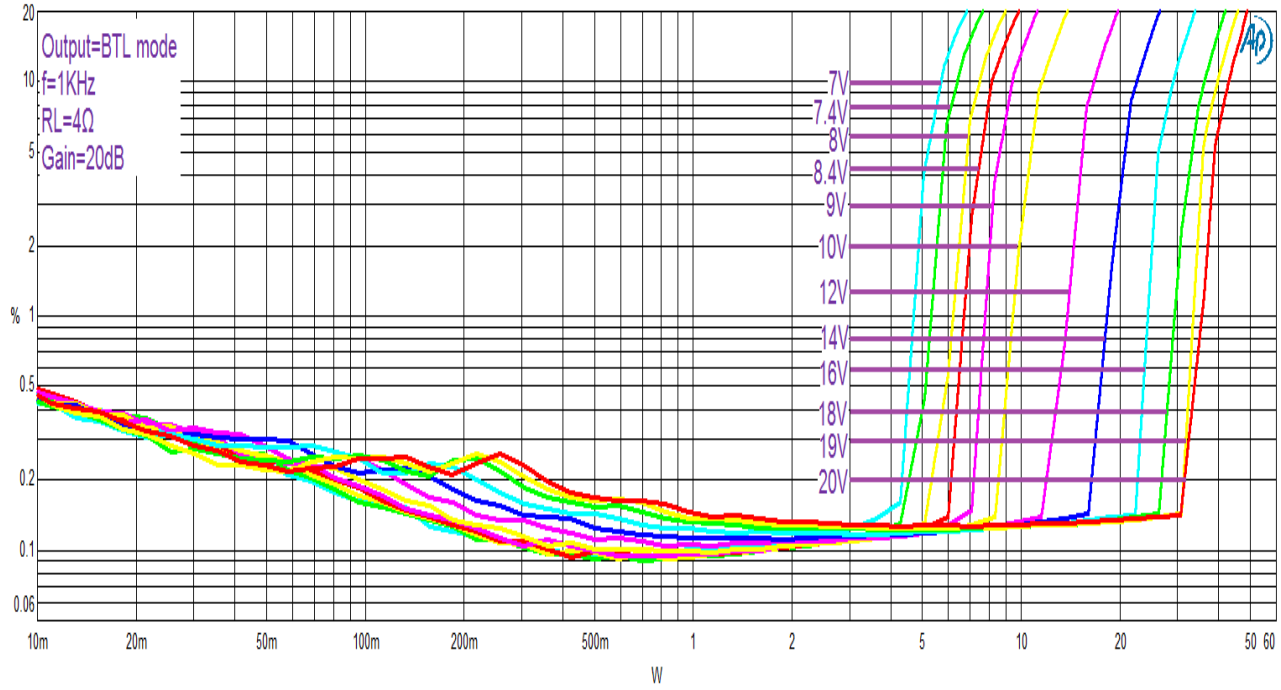


Figure 6
THD+N vs. Output Power (@ Output type=BTL Mode, **RL=8Ω**, f=1kHz, Gain=20, 2 Channel. Test)

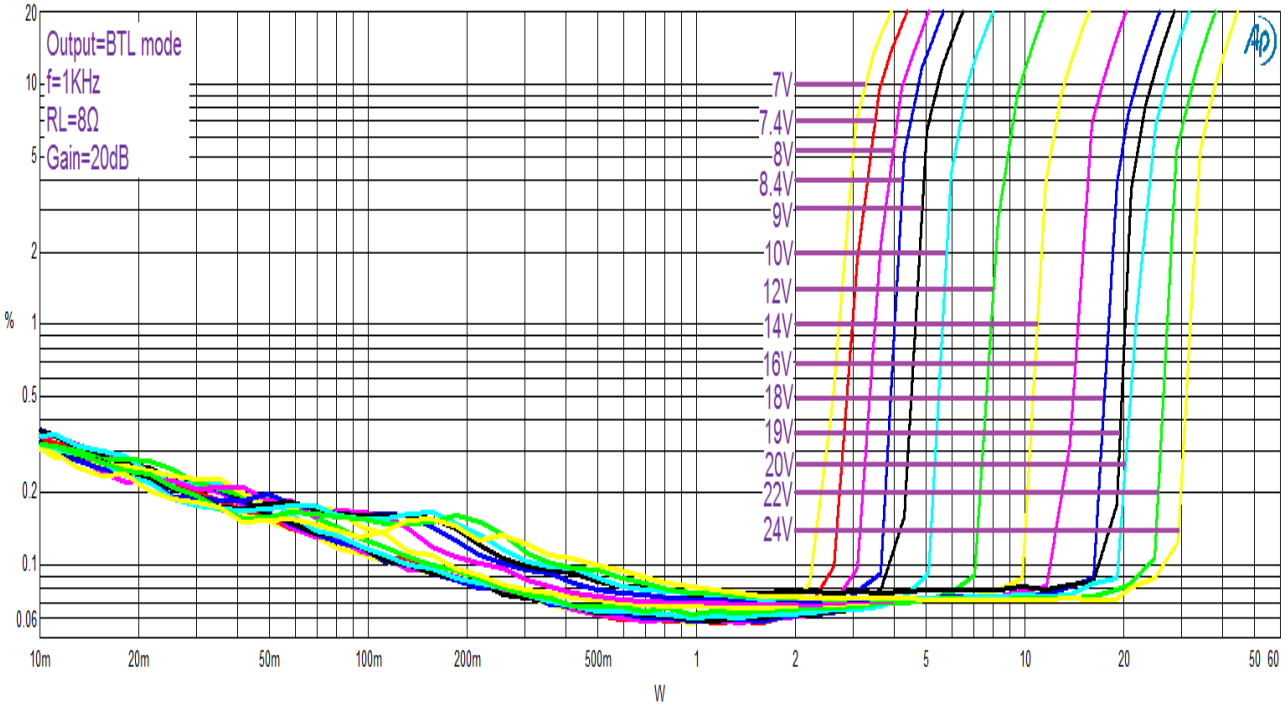


Figure 7
THD+N vs. Output Power (@ Output type=SE Mode, **RL=4Ω**, f=1kHz, Gain=20, 4 Channel. Test)

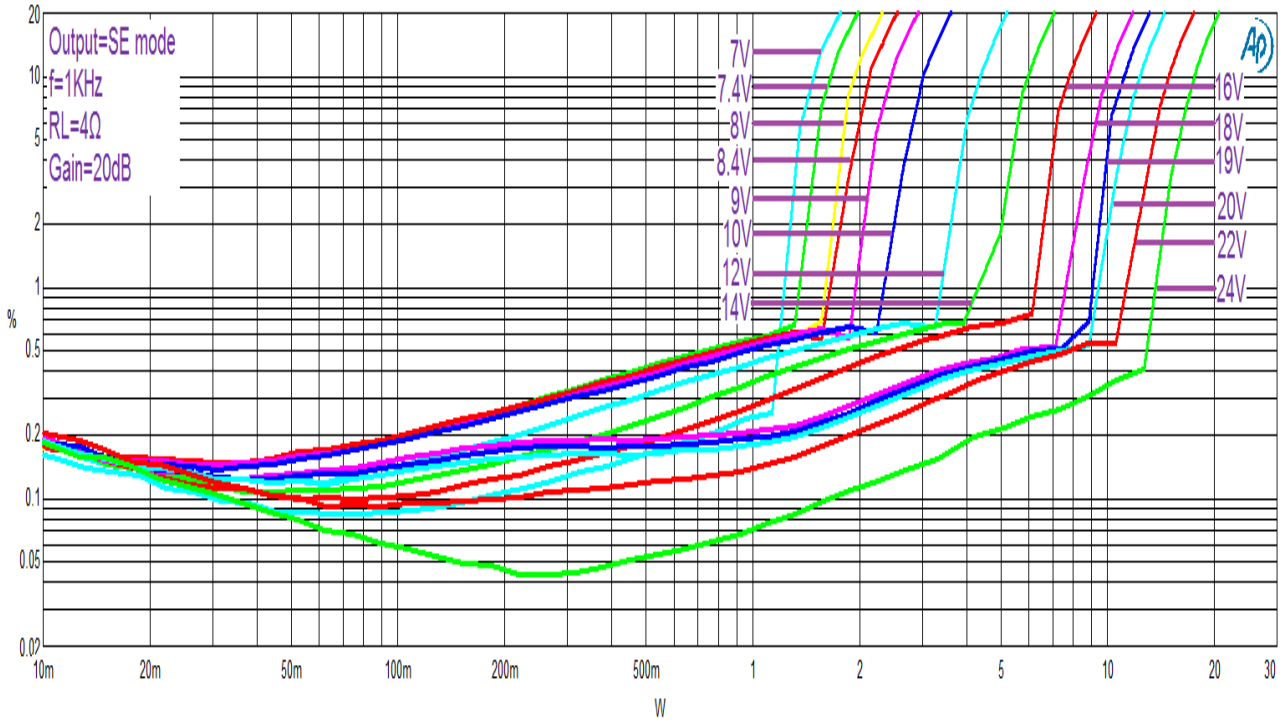


Figure 8
THD+N vs. Output Power (@ Output type=SE Mode, **RL=8Ω**, f=1kHz, Gain=20, 4 Channel. Test)

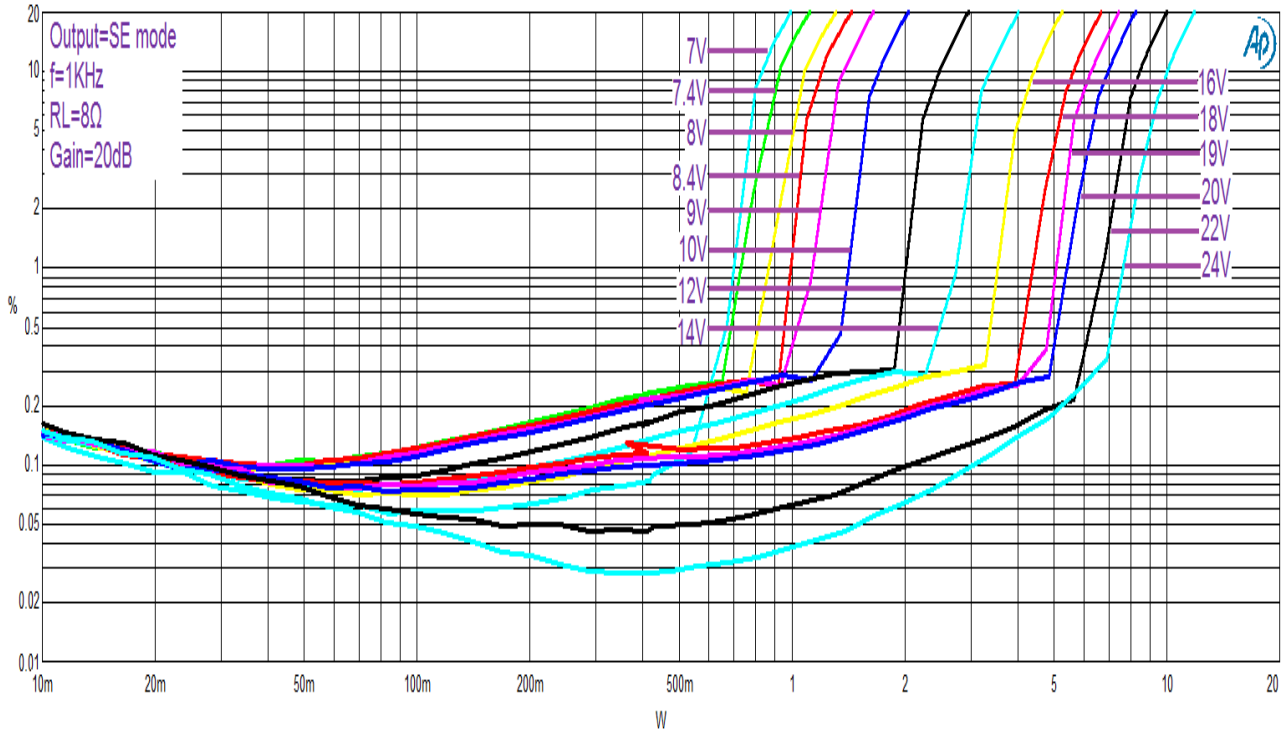


Figure 9
THD+N vs. Output Power (@ Output type=PBTL Mode, **RL=2Ω**, f=1kHz, Gain=20)

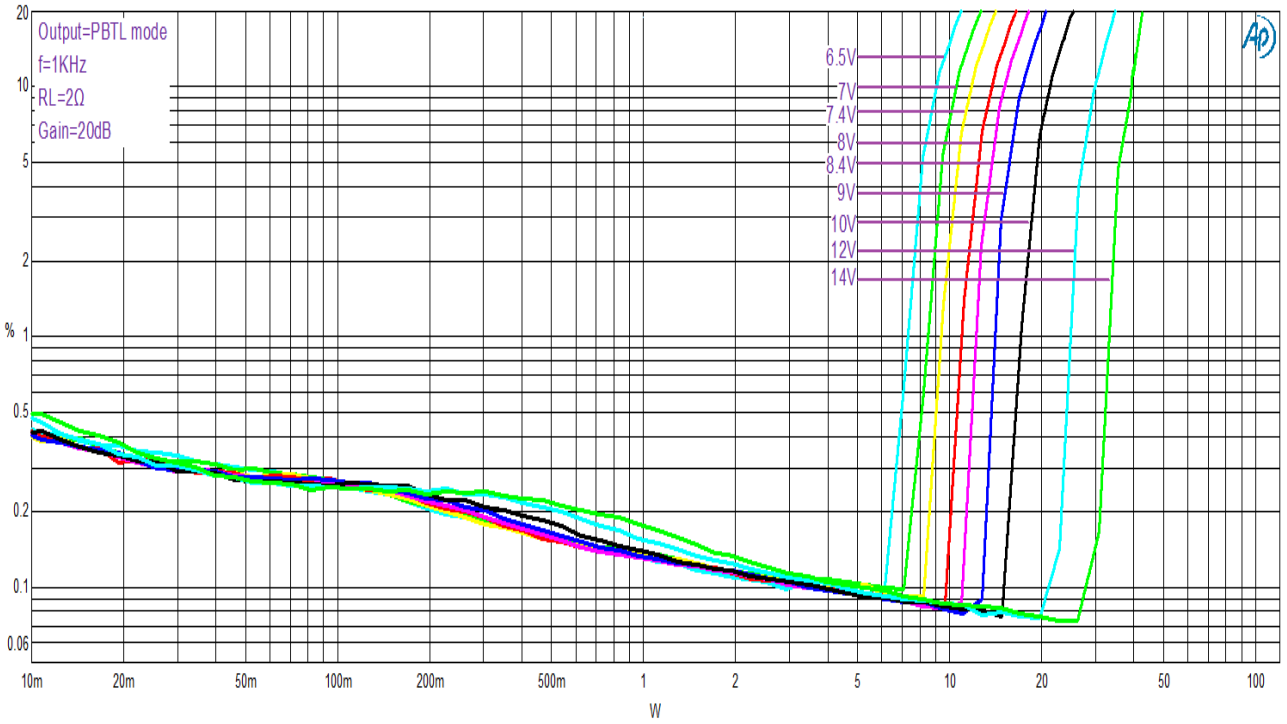


Figure 10
THD+N vs. Output Power (@ Output type=PBTL Mode, **RL=3Ω**, f=1kHz, Gain=20)

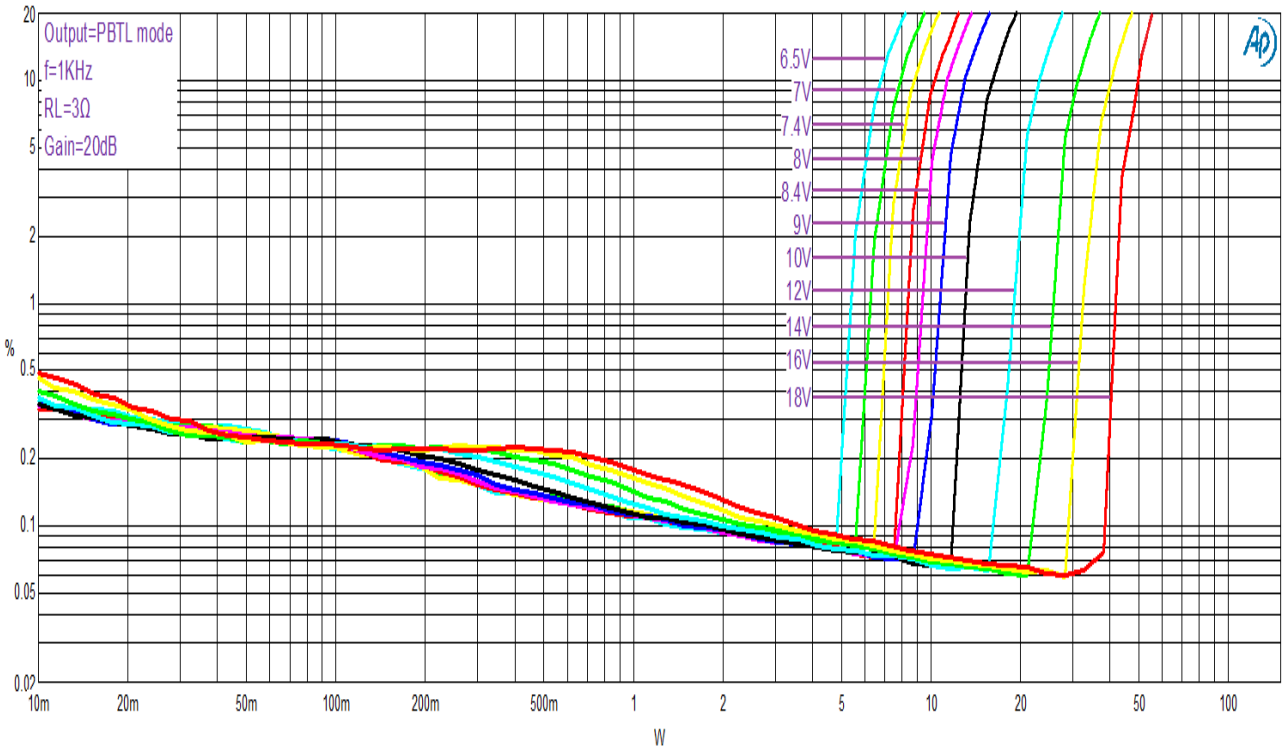


Figure 11
THD+N vs. Output Power (@ Output type=PBTL Mode, **RL=4Ω**, f=1kHz, Gain=20)

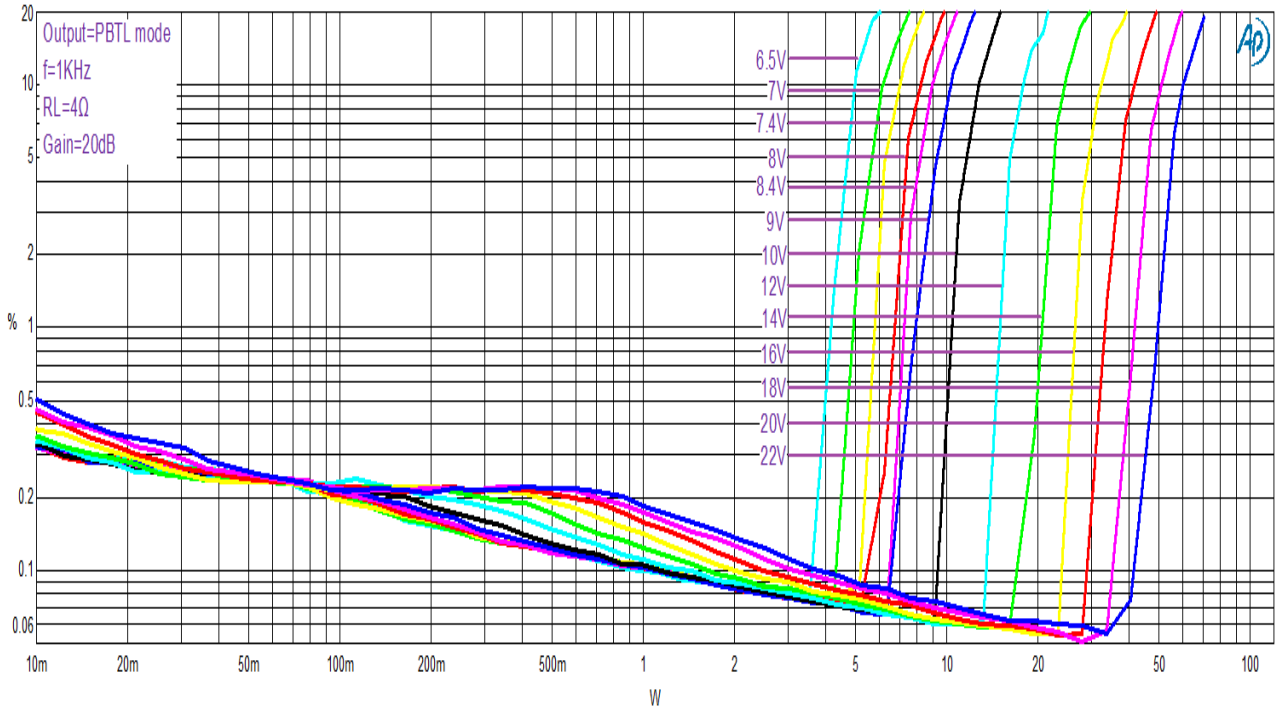


Figure 12
Supply ripple rejection (Ksvr, **RL=4Ω**, BTL mode)

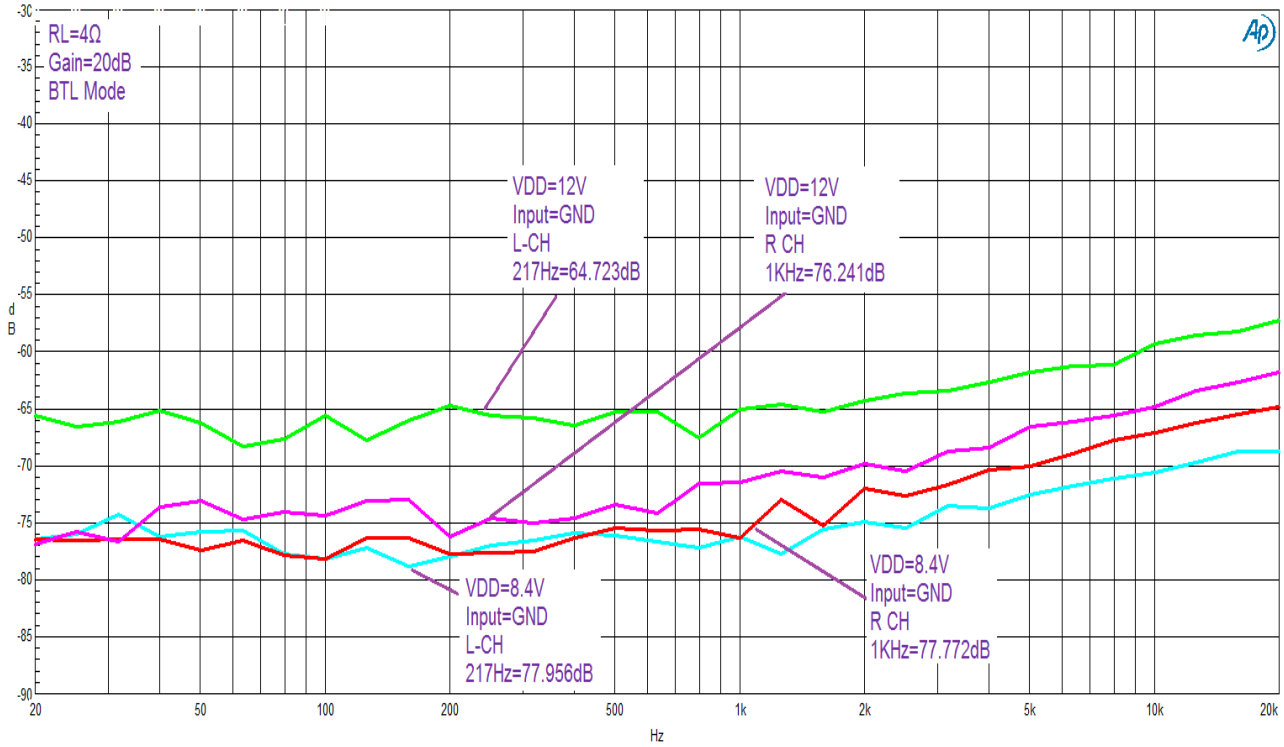


Figure 13
SNR vs. Noise Level (Input=Floating / BTL mode)

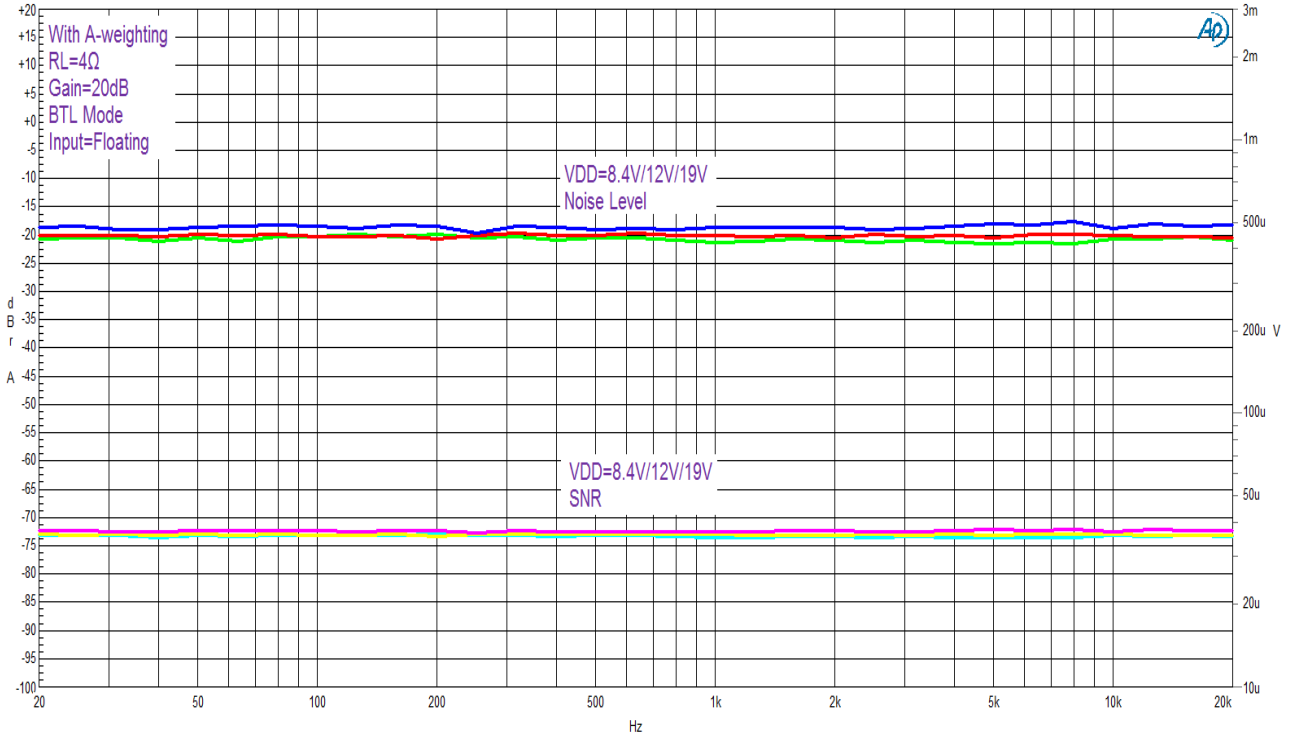


Figure 14
SNR vs. Noise Level (Input=GND / BTL mode)

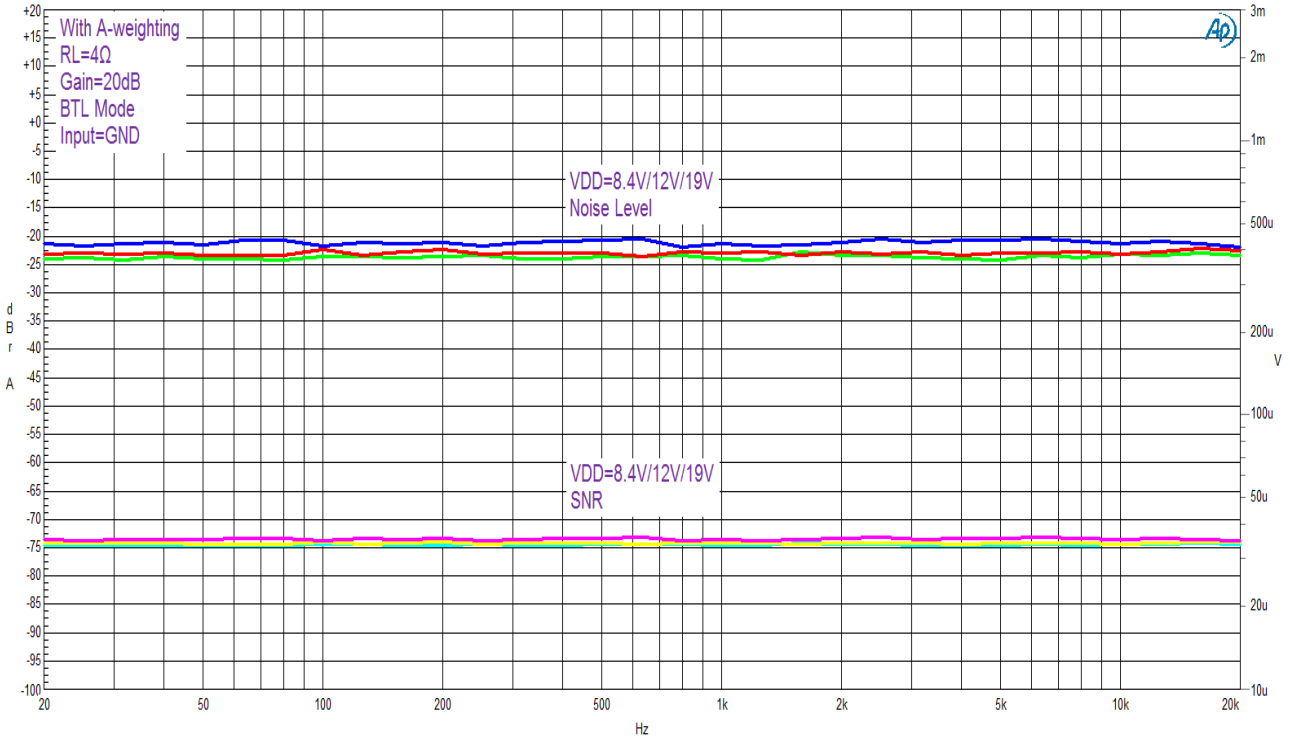


Figure 15
Crosstalk vs. Frequency (BTL mode, L to R)

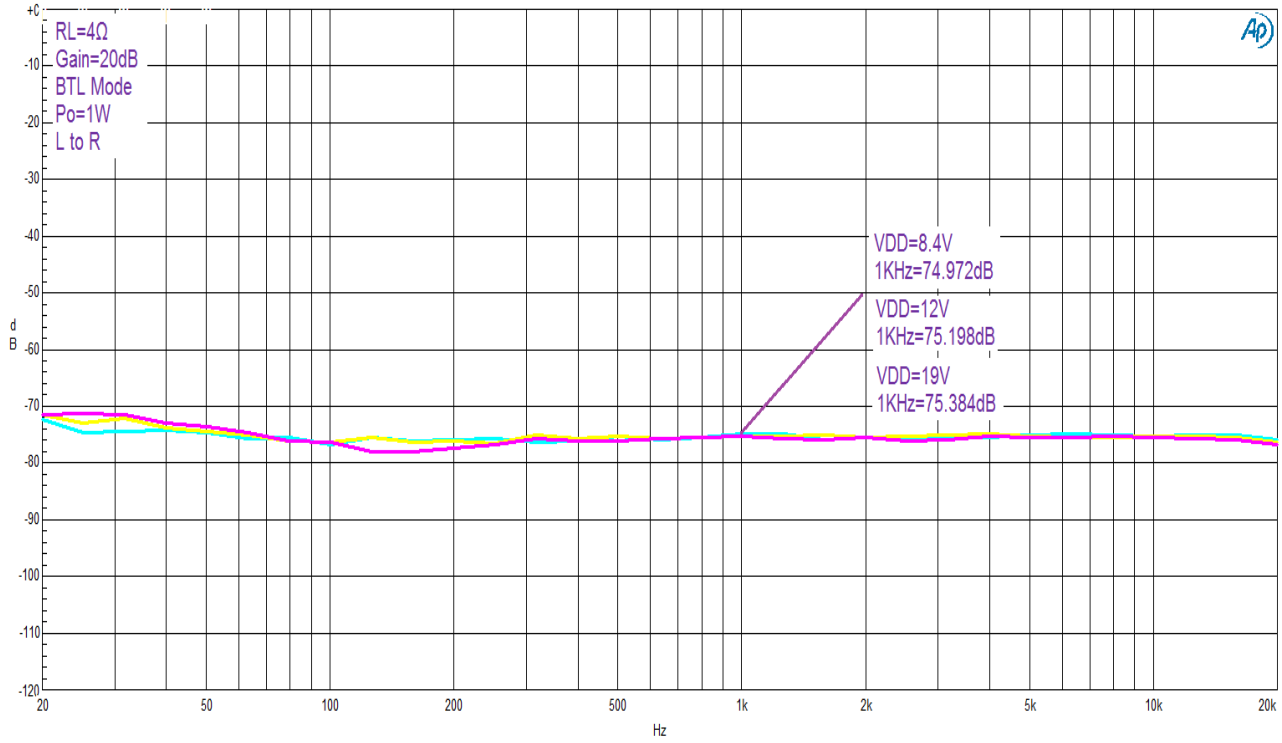
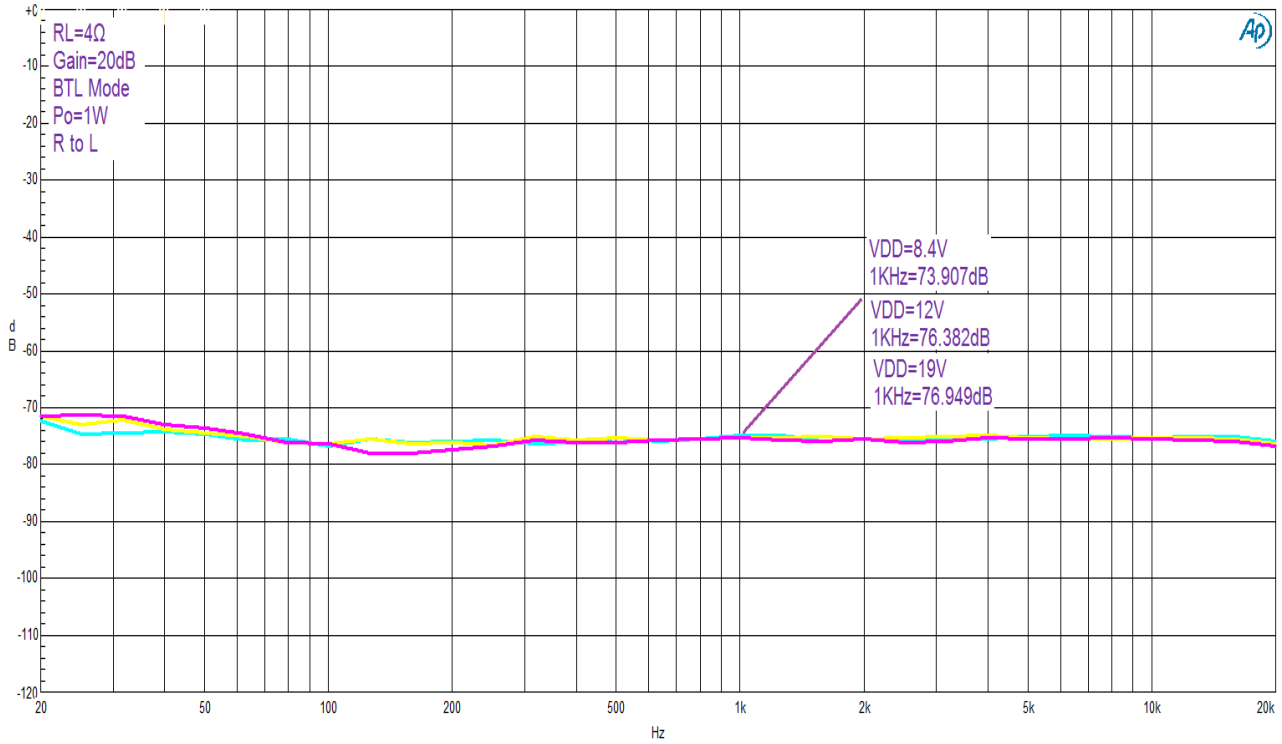
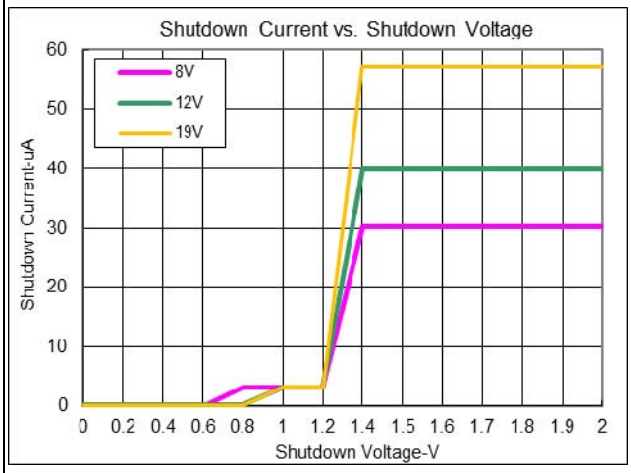


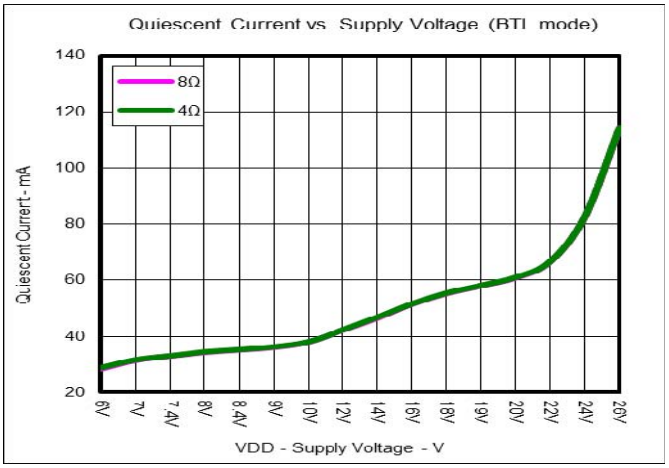
Figure 16
Crosstalk vs. Frequency (BTL mode, R to L)



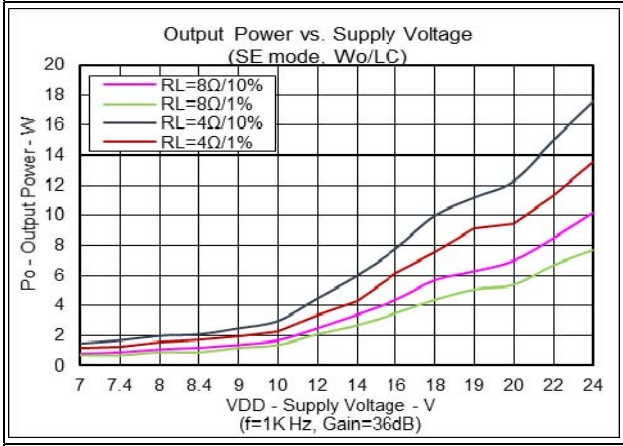
SD Current vs. SD Voltage



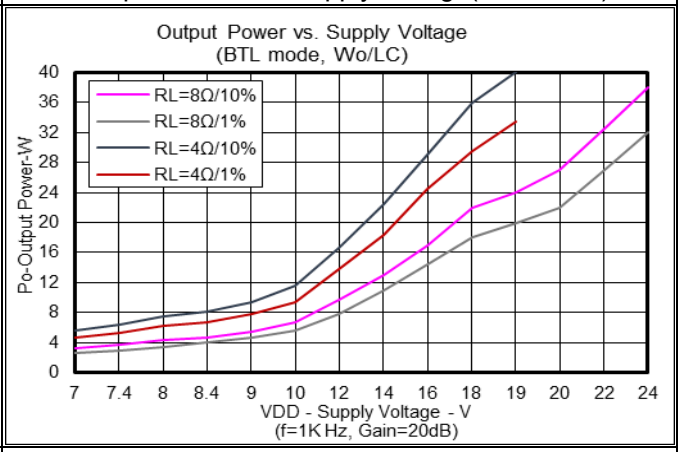
Quiescent Current vs. Supply voltage (BTL mode)



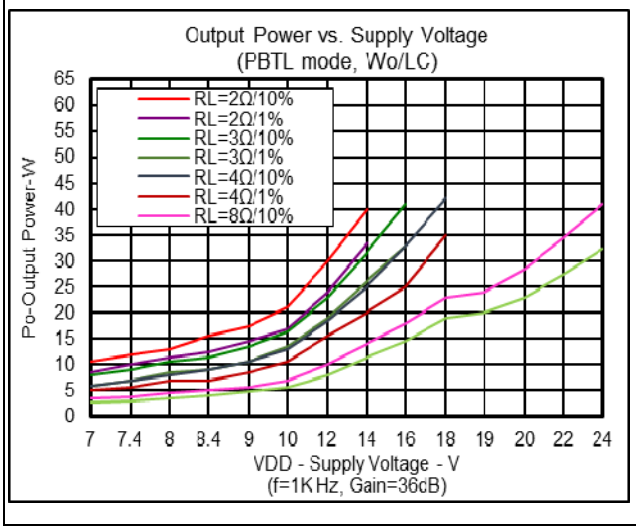
Output Power vs. Supply Voltage(SE mode))



Output Power vs. Supply Voltage(BTL mode)



Output Power vs. Supply Voltage(PBTL mode)



▪ APPLICATION INFORMATION

Input Capacitors (Ci)

In typical application, C_i and the input resistance of the amplifier (R_i) form a high-pass filter with the corner frequency(f_c) determined in equation.

$$f_c = 1 / (2\pi R_i C_i)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit.

For example

If the gain is known and is constant, use Ri from Table 1 to calculate Ci and use below equation.

$$C_i = 1 / (2\pi R_i f_c)$$

A.) If R_i is 36dB(8.2 kΩ) and the specification calls for a flat bass response down to 20 Hz.

Ci = 1 / (2π x 8.2KΩ x 20Hz)=0.9705uF，One would likely choose a value of 1.0uF as this value is commonly used.

B.) If R_i is 32dB(12.5 kΩ) and the specification calls for a flat bass response down to 20 Hz.

Ci = 1 / (2π x 12.5KΩ x 20Hz)=0.6366uF，One would likely choose a value of 0.68uF as this value is commonly used.

C.) If R_i is 26dB(25 kΩ) and the specification calls for a flat bass response down to 20 Hz.

Ci = 1 / (2π x 25KΩ x 20Hz)=0.3183uF，One would likely choose a value of 0.33uF as this value is commonly used.

D.) If R_i is 20dB(50 kΩ) and the specification calls for a flat bass response down to 20 Hz.

Ci = 1 / (2π x 50KΩ x 20Hz)=0.1592uF，One would likely choose a value of 0.15uF as this value is commonly used.

Input Resistors (Ri) and Gain

The LY8322 support four type digital gain selectable. So changing the gain setting can vary the input resistance of the amplifier from 8.2 kΩ ±20% to 50 kΩ ±20%. As a result, cutoff frequency may change when changing gain steps. (Reference table 1)

Gain setting (GAIN0 and GAIN1)

The gain of the LY8322 is set by two input pins, GAIN0 and GAIN1.

Table 1. Gain Setting

Gain0	Gain1	Amplifier Gain (dB) TYP.	Input Impedance (KΩ)
0	0	36	8.2
0	1	32	12.5
1	0	26	25
1	1	20	50

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small.

However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input impedance.
For design purposes, the input resistance should be designed assuming an input impedance of 6.6 kΩ, which is the absolute minimum input impedance of the LY8322. At the lower gain settings, the input impedance could increase as high as 60 kΩ.

Mode Select

The LY8322 offers the feature of 4 type mode select. Through the pin 12 connection as the following for mode selection.

Table 2. Output Mode Select Table

Mode pin (pin 12)	Mode
0Ω to GND	BTLx2
30KΩ to GND	2.1 CH
120KΩ to GND	SEx4
0Ω to GVDD	PBTLx1

Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the LY8322 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the LY8322 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance.
For good transient performance, the impedance seen at each of the two differential inputs should be the same. The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the more power-up time (ms). If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the control pin voltage divider circuit. Add a 1μF capacitor to ground at this pin.

Bypass Capacitor (Cbypass)

The Bypass Capacitor (C3) is the most critical capacitor and serves important functions. During start-up or recovery from shutdown mode, Cbypass determines the rate at which the amplifier starts up. The Cbypass will to reduce noise caused by the power supply coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded the PSRR and THD+N values. The bypass capacitor (C3) with values of 0.1μF to 4.7μF is recommended for the best THD and noise performance. Therefore, increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

Power Supply Decoupling Capacitor (Cs)

The LY8322 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1uF~1.0uF, placed as close as possible to the device PVCC lead works best. Placing this decoupling capacitor close to the LY8322 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 470uF or greater capacitor placed near the audio power amplifier would also help, so 470uF or larger capacitor should be placed on each PVCC terminal.

BST Capacitors

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 1.0uF ceramic capacitor, rated for at least 25V up, must be connected from each output to its corresponding bootstrap input. Specifically, all 1.0uF capacitor must be connected from OUT to BST pin.
The bootstrap capacitors connected between the BST pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Shutdown Function

When the LY8322 not in use. The device will be to turn off the amplifier to reduce power consumption.
When logic **low** is applied to the shutdown pin, this shutdown feature will turns the amplifier off. By switching the shutdown pin connected to GND, the device supply current draw will be minimized in idle mode. The pin cannot be left floating due to the internal did not pull-up.

Mute Function

The Mute pin is an input pin to control the LY8322 output state. A logic **high** is disable the LY8322 outputs. A logic **low** on this pin enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a TV or transitioning between different audio sources.
The Mute pin should never be left floating. For power conservation, the SD pin should be used to reduce the quiescent current to the absolute minimum level.

Over-Heat Protection

The LY8322 has a built-in over-heat protection circuit, it will turn off all power output when the chip temperature over 165℃, (There is a ±15°C tolerance on this trip point from device to device.) the chip will return to normal operation automatically after the temperature cool down to 110℃.
Thermal protection faults are NOT reported on the FAULT pin.

Short Circuit Protection and Automatic Recovery Feature

The LY8322 has short circuit protection circuitry on the outputs that prevents damage to the device during output-pin to-output pin shorts. When the short circuit is detected on the outputs, the part immediately goes into shutdown. This is a latched fault and must be reset by cycling the voltage on the shutdown pin to a logic low and back to the logic high, or by cycling the power off and then back on. This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry activates again.
If automatic recovery from the short circuit protection latch is desired, connect the FAULT pin directly to the SD pin. This allows the FAULT pin function to automatically drive the SD pin low which clears the short-circuit protection latch.

Power Limit

The voltage at PLIMIT pin can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required.

Table 3. PLIMIT Voltage vs. Output Power Table

Test Condition	PLIMIT Voltage (V)	Output power (W)	PLIMIT Voltage (V)	Output Voltage (W)
	RL=4Ω		RL=8Ω	
Pvcc=19V, Gain=20dB	2	14.5	1	24.5
Pvcc=12V, Gain=20dB	1	16.5	1	9.7
Pvcc=8.4V, Gain20dB	1	8.2	1	4.7

Single-Ended Output Capacitor Select, (C_O)

In single-ended (SE) applications, the dc blocking capacitor forms a high-pass filter with the speaker impedance. The frequency response rolls off with decreasing frequency at a rate of 20 dB/decade. The cutoff frequency is determined by :

$fc = 1 / (2\pi R_L C_O)$

Table 4. Filter Responses Reference Values

Speaker Load R_L (Ω)	SE mode - Co Capacitor select(uF)						
	fc=180Hz	fc=120Hz	fc=100Hz	fc=80Hz	fc=60Hz	fc=40Hz	fc=20Hz
4	220	330	390	470	680	1000	2200
6	-	220	-	330	470	680	1500
8	-	-	200	-	330	470	1000

BTL Output (Use an Output Filter for EMI Suppression)

The LY8322 has been tested with a simple ferrite bead filter for some applications. And it is passes FCC Class B specifications under these conditions using 25cm twisted speaker wires.

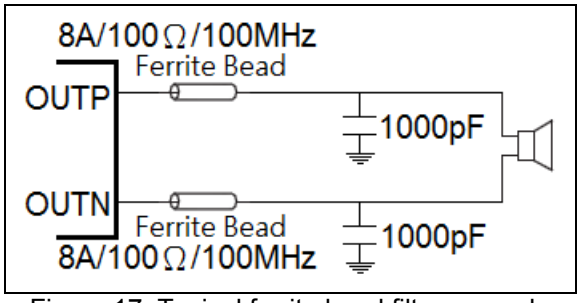


Figure 17. Typical ferrite bead filter example

If there are nearby circuits which are sensitive to noise or there need long speaker wires. It is necessary to add a complete LC reconstruction filter.

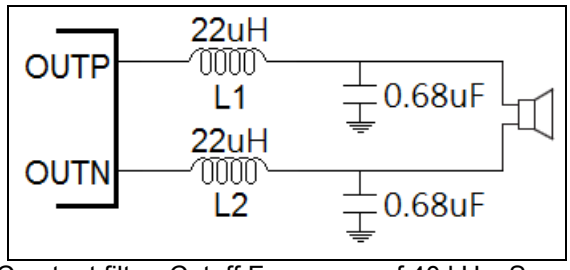


Figure 18. Typical LC output filter, Cutoff Frequency of 40 kHz, Speaker Impedance = 4Ω

The cutoff frequency is determined by :

$fc = 1 / (2\pi * SQRT(LC))$

Ferrite Bead Filter Considerations

Using the Advanced EMI Suppression Technology in the LY8322 amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible with a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class D amplifier. And it is important that the ferrite bead is large current enough to maintain its impedance at the peak currents expected for the amplifier. Also, high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

PCB Layout

Because the LY8322 is a class-D amplifier that switches at a high frequency, the layout of the PCB should be optimized according to the following guidelines for the best possible performance.

1. Thermal pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability.
2. Decoupling capacitors—The high-frequency 0.1uF decoupling capacitors should be placed as close to the PVCC pins and AVCC pin terminals as possible.
   And the Bypass pin capacitor should also be placed as close to the device as possible.
   Large (470uF or greater) bulk power-supply decoupling capacitors should be placed near the device on the PVCC terminals.
3. Grounding—The AVCC pin decoupling capacitor and Bypass pin capacitor should each be grounded to analog ground (AGND).
   The PVCC decoupling capacitors should each be grounded to power ground (PGND). Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the LY8322.
4. Output filter—The reconstruction filter should be placed as close to the output terminals as possible for the best EMI performance. The capacitors should be grounded to power ground.
5. The input resistors need to be very close to the device input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the device.
6. Making the high current traces going to PVCC, GND, V_{O+} and V_{O-} pins of the device should be as wide as possible to minimize trace resistance. If these traces are too thin, the device's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

▪ DEMO BOARD INFORMATION

Demo Board Application Circuit (BTLx2 mode)

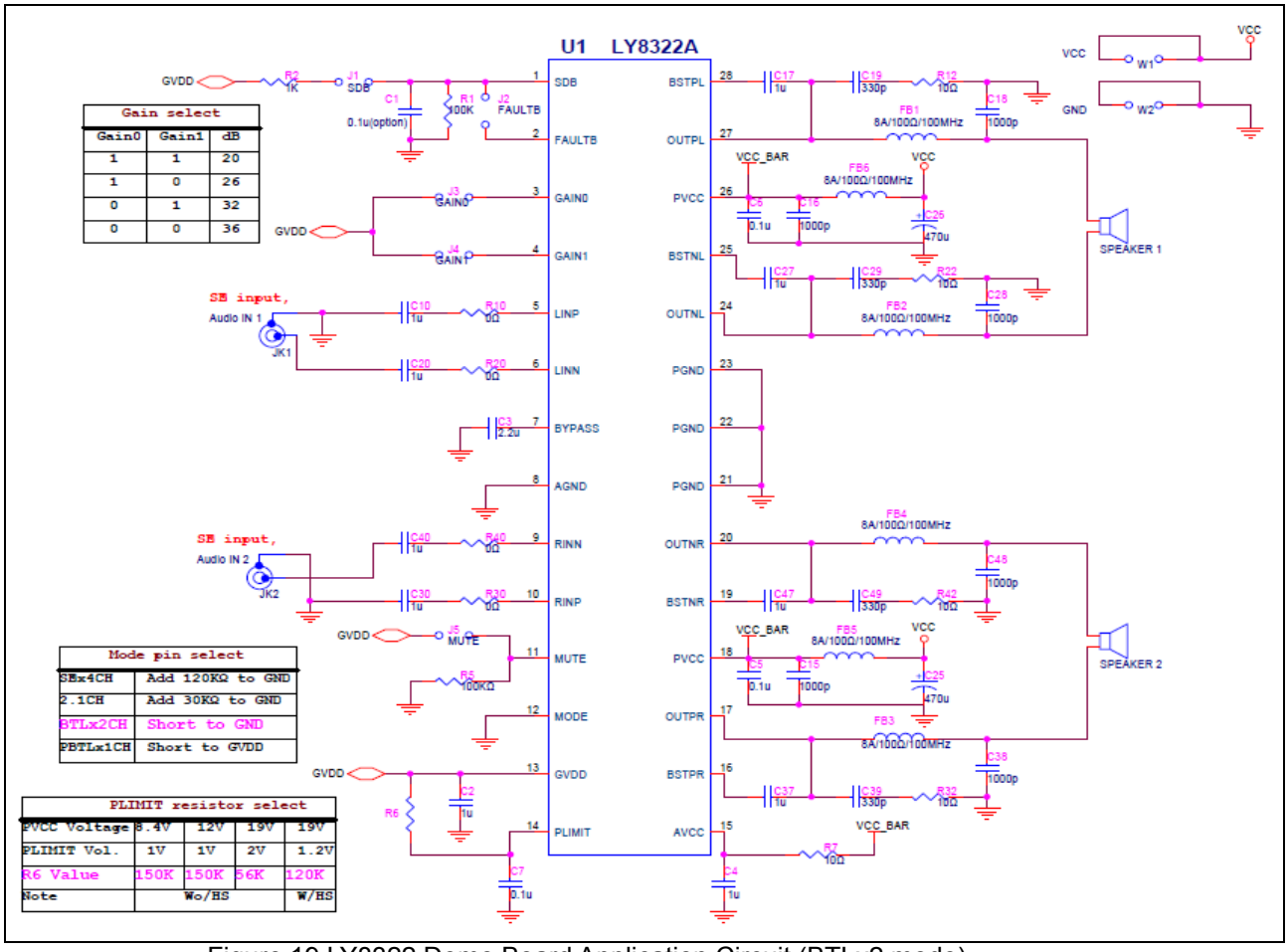


Figure 19 LY8322 Demo Board Application Circuit (BTLx2 mode)

Demo Board BOM List (BTLx2 mode)

LY8322, BTLx2 V2.2 BOM List

No.	Part No.	Reference	QTY	Description	Note
1	IC, LY8322A	U1	1	CLASS-D Audio AMP, TSSOP28EP	
2	Capacitor,470uF	C25,C26	2	35V,105℃,10*20,EC Cap.	
3	Capacitor, 0.1uF	C5,C6	2	SMD0805,CER,80%/-20%	
4	Capacitor, 1uF	C2,C4,C10,C20,C30,C40,C17, C27,C37,C47	10	SMD0805 ,CER,80%/-20%	
5	Capacitor, 2.2uF	C3	1	SMD0805 ,CER,80%/-20%	
6	Capacitor, 1000pF	C15,C16,C18,C28,C38,C48	6	SMD0805 ,CER,80%/-20%	4ea option
7	Capacitor, 330pF	C19,C29,C39,C49	4	SMD0805 ,CER,80%/-20%	option
8	Resistor,	R6	1	SMD0805,1/8W, 1%	PL. Table
9	Resistor, 100KΩ	R1,R5	2	SMD0805,1/8W, 1%	
10	Resistor, 1KΩ	R2	1	SMD0805,1/8W, 1%	
11	Resistor, 10Ω	R7,R12,R22,R32,R42	5	SMD0805,1/8W, 1%	4ea, option
12	Ferrite Bead	FB1,FB2,FB3,FB4,FB5,FB6	6	SMD1812,8A/100Ω/100Mhz	option

Demo Board Application Circuit (SEx4 mode)

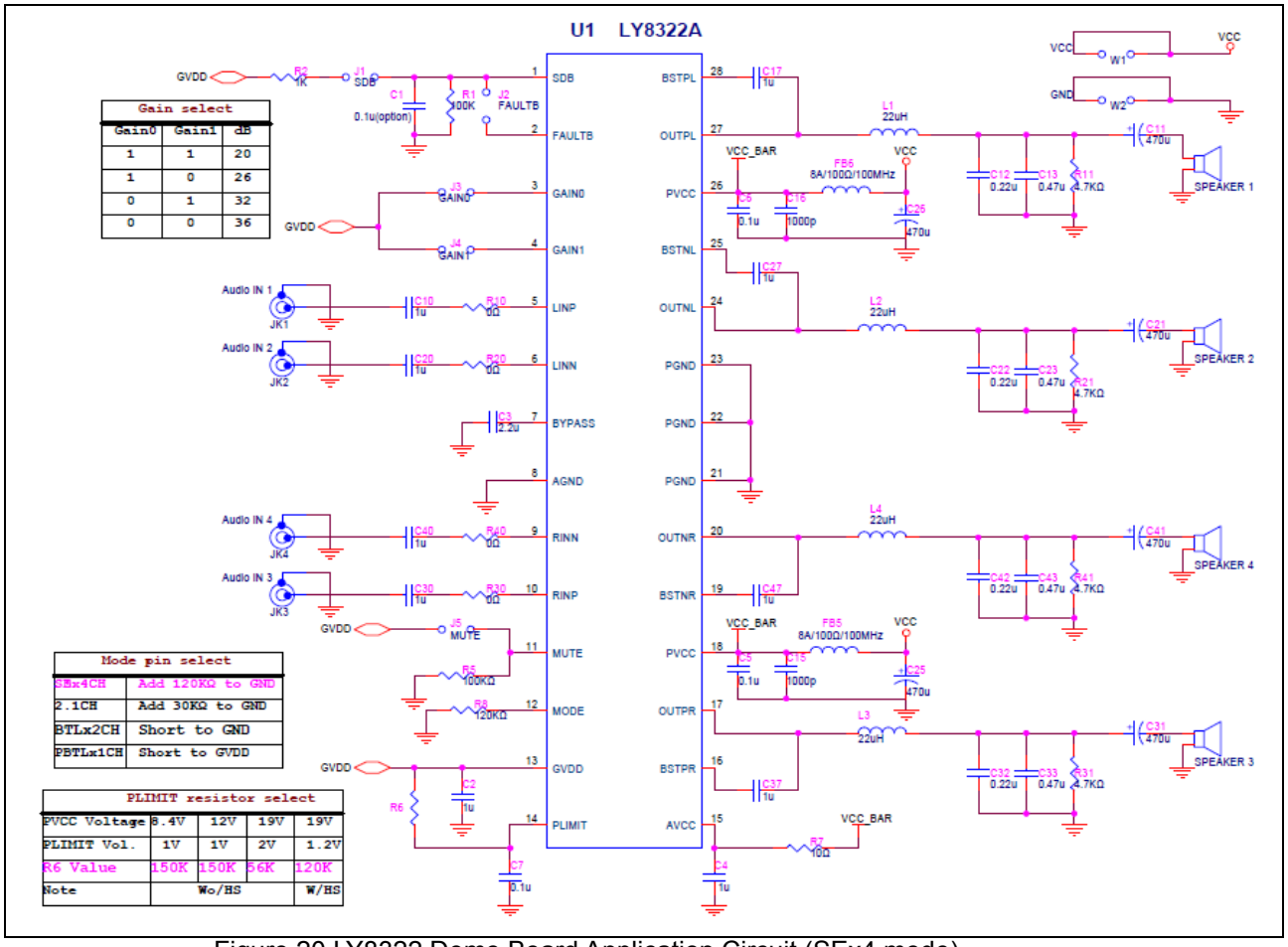


Figure 20 LY8322 Demo Board Application Circuit (SEx4 mode)

Demo Board BOM List (SEx4 mode)

LY8322, SEx4 V2.2 BOM List

No.	Part No.	Reference	QTY	Description	Note
1	IC, LY8322A	U1	1	CLASS-D Audio AMP, TSSOP28EP	
2	Capacitor,470uF	C25,C26,C11,C21,C31,C41	6	35V,105℃,10*20,EC Cap.	
3	Capacitor, 0.1uF	C5,C6	2	SMD0805,CER,80%/-20%	
4	Capacitor, 1uF	C2,C4,C10,C20,C30,C40,C17, C27,C37,C47	10	SMD0805 ,CER,80%/-20%	
5	Capacitor, 2.2uF	C3	1	SMD0805 ,CER,80%/-20%	
6	Capacitor, 1000pF	C15,C16,	2	SMD0805 ,CER,80%/-20%	
7	Capacitor, 0.47uF	C13,C23,C33,C43	4	SMD0805 ,CER,80%/-20%	SE only
8	Capacitor, 0.22uF	C12,C22,C32,C42	4	SMD0805 ,CER,80%/-20%	SE only
9	Resistor	R6	1	SMD0805,1/8W, 1%	PL. Table
10	Resistor, 120KΩ	R8	1	SMD0805,1/8W, 1%	
11	Resistor, 100KΩ	R1,R5	4	SMD0805,1/8W, 1%	
12	Resistor, 4.7KΩ	R11,R21,R31,R41	4	SMD0805,1/8W, 1%	
13	Resistor, 1KΩ	R2	1	SMD0805,1/8W, 1%	
14	Resistor, 10Ω	R7	1	SMD0805,1/8W, 1%	
15	Ferrite Bead	FB1,FB2	2	SMD1812,8A/100Ω/100Mhz	option
16	Inductors 22uH	L1, L2, L3, L4	4	DIP, TOKO (A7502BY-220M)	SE only

Demo Board Application Circuit (2.1CH mode)

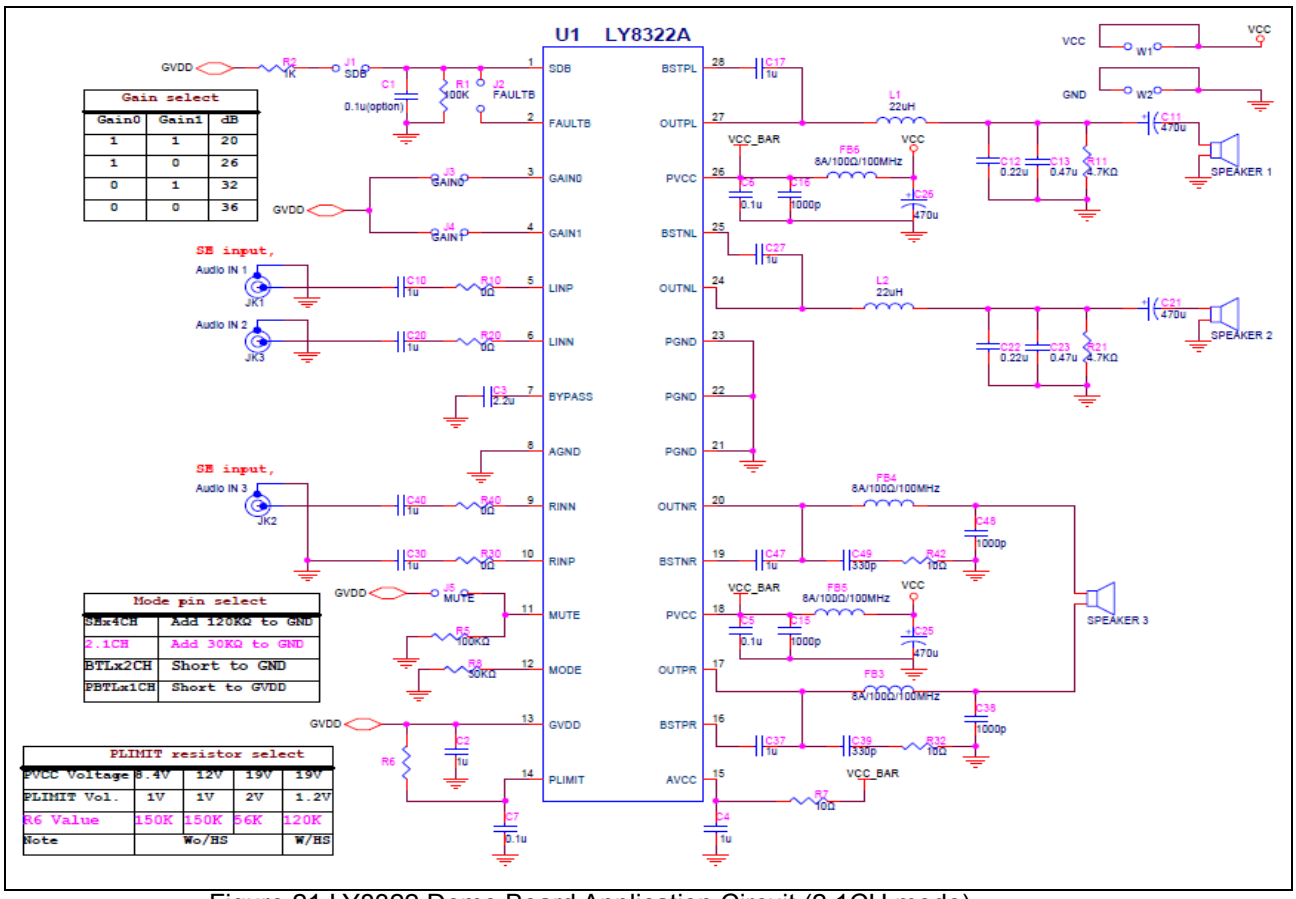


Figure 21 LY8322 Demo Board Application Circuit (2.1CH mode)

Demo Board BOM List (2.1CH mode)

LY8322, 2.1CH V2.2 BOM List

No.	Part No.	Reference	QTY	Description	Note
1	IC, LY8322A	U1	1	CLASS-D Audio AMP, TSSOP28EP	
2	Capacitor,470uF	C25,C26,C11,C21	4	35V,105℃,10*20,EC Cap.	
3	Capacitor, 0.1uF	C5,C6	2	SMD0805,CER,80%/-20%	
4	Capacitor, 1uF	C2,C4,C10,C20,C30,C40,C17, C27,C37,C47	10	SMD0805 ,CER,80%/-20%	
5	Capacitor, 2.2uF	C3	1	SMD0805 ,CER,80%/-20%	
6	Capacitor, 1000pF	C15,C16,C38,C48	4	SMD0805 ,CER,80%/-20%	2ea, option
7	Capacitor, 330pF	C39,C49	2	SMD0805 ,CER,80%/-20%	option
8	Capacitor, 0.22uF	C12,C22	2	SMD0805 ,CER,80%/-20%	SE only
9	Capacitor, 0.47uF	C13,C23	2	SMD0805 ,CER,80%/-20%	SE only
10	Resistor	R6	1	SMD0805,1/8W, 1%	PL. Table
11	Resistor, 30KΩ	R8	1	SMD0805,1/8W, 1%	
12	Resistor, 100KΩ	R1,R5	2	SMD0805,1/8W, 1%	
13	Resistor, 4.7KΩ	R11,R21	2	SMD0805,1/8W, 1%	
14	Resistor, 1KΩ	R2	1	SMD0805,1/8W, 1%	
15	Resistor, 10Ω	R7,R32,R42	3	SMD0805,1/8W, 1%	2ea, option
16	Ferrite Bead	FB3,FB4,FB5,FB6	4	SMD1812,8A/100Ω/100Mhz	option
17	Inductors 22uH	L1, L2	2	DIP, TOKO (A7502BY-220M)	SE only

Demo Board Application Circuit (PBTLx1 mode)

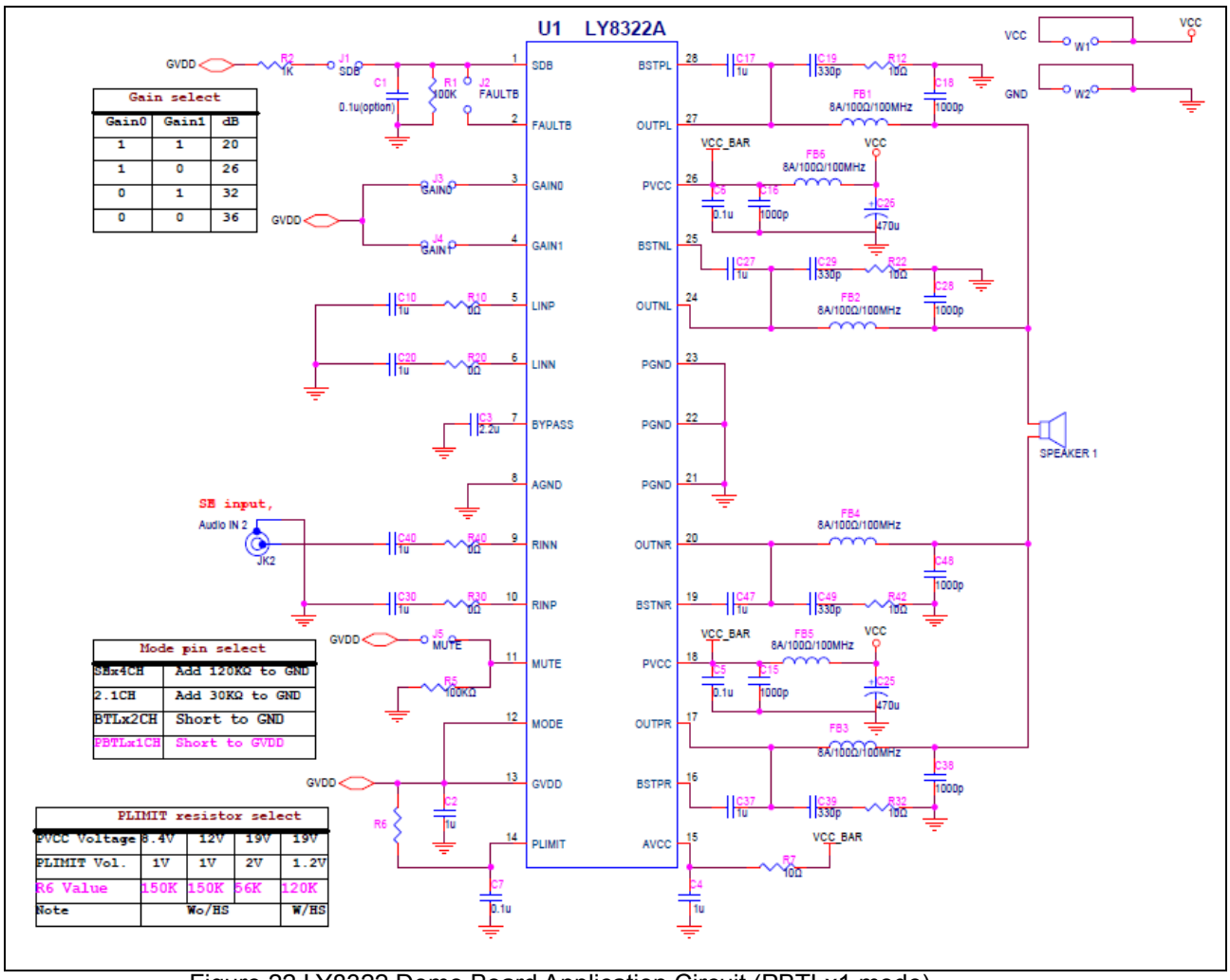


Figure 22 LY8322 Demo Board Application Circuit (PBTLx1 mode)

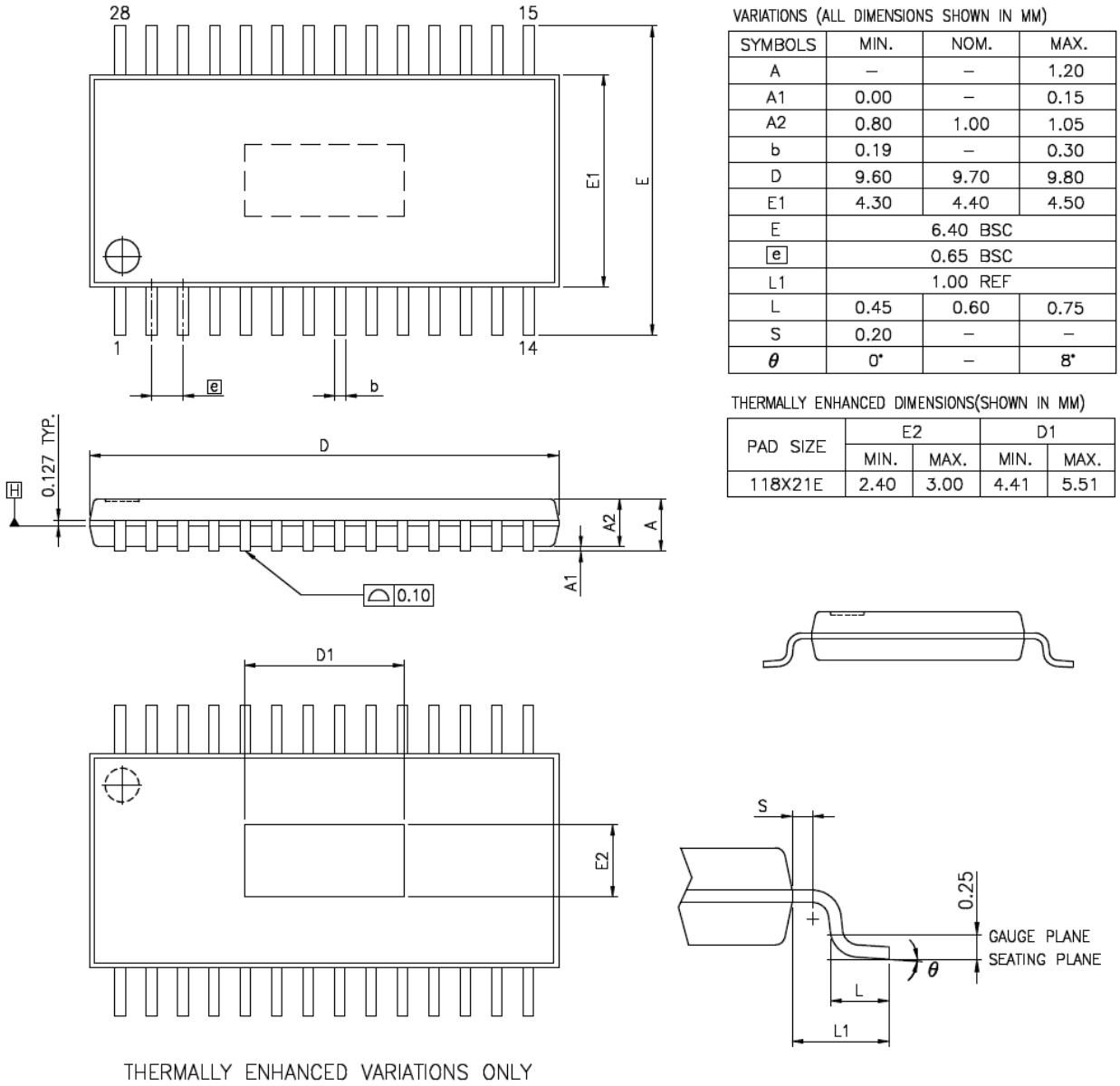
Demo Board BOM List (PBTLx1 mode)

LY8322, PBTLx1 V2.2 BOM List

No.	Part No.	Reference	QTY	Description	Note
1	IC, LY8322A	U1	1	CLASS-D Audio AMP, TSSOP28EP	
2	Capacitor,470uF	C25,C26	2	35V,105℃,10*20,EC Cap.	
3	Capacitor, 0.1uF	C5,C6	2	SMD0805,CER,80%/-20%	
4	Capacitor, 1uF	C2,C4,C10,C20,C30,C40,C17, C27,C37,C47	10	SMD0805 ,CER,80%/-20%	
5	Capacitor, 2.2uF	C3	1	SMD0805 ,CER,80%/-20%	
6	Capacitor, 1000pF	C15,C16,C18,C28,C38,C48	6	SMD0805 ,CER,80%/-20%	4ea, option
7	Capacitor, 330pF	C19,C29,C39,C49	4	SMD0805 ,CER,80%/-20%	option
8	Resistor	R6	1	SMD0805,1/8W, 1%	PL. Table
9	Resistor, 100KΩ	R1,R5	2	SMD0805,1/8W, 1%	
10	Resistor, 1KΩ	R2	1	SMD0805,1/8W, 1%	
11	Resistor, 10Ω	R7,R12,R22,R32,R42	5	SMD0805,1/8W, 1%	4ea, option
12	Ferrite Bead	FB1,FB2,FB3,FB4,FB5,FB6	6	SMD1812,8A/100Ω/100Mhz	option

PACKAGE OUTLINE DIMENSION

TSSOP 28 Pin Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
118X21E	2.40	3.00	4.41	5.51